# PhD Defence <br> Soutenance de Doctorat Automata on Timed Structures 

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## Heater Monitoring



## Heater Monitoring



## Heater Monitoring



## Heater Monitoring



## Modeling

## States of the Heater



heating

doing nothing

## Modeling



## Modeling



## Modeling


abnormaly heating out of order

## Modeling



## Modeling



## Executions in the Model



## Executions in the Model



## Executions in the Model



## Executions in the Model



## Diagnosis



## Diagnosis



1•on•3•n
safe
faulty


## Diagnosis



1-on•3•on


## Diagnosis



1•on•3. on.8


## Diagnosis



1•n•3. on•8


## Diagnosis



1•on•3.on•8•on
safe
faulty


## Diagnosis



## Weakness of Times Automata



Figure: A non-determinizable timed automaton [AD94]


Figure: Timed automaton where $\epsilon$-transitions can't be removed [BDGP98]

## My Work

- Step 1 : Determinization - General Powerset Construction
- Definition of an adapted model - Automata on Timed Structures
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- Relations between the new powerset construction and previous determinization results


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- Step 3 : Implementation - The power of precomputation
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- Comparison of the performance.


## General Idea



Discrete System


Dynamic System

## General Idea

## Updates



Constraints

## General Idea

## Updates



Constraints

## Timed Domains

Une horloge donne l'heure, nous sommes bien d'accord, elle passe même ses heures à ne faire que cela, mais elle ne montre rien de ce qu'est le temps en amont de ce processus d'actualisation. Elle dissimule plutôt le temps derrière le masque convaincant d'une mobilité parfaitement régulière. - Etienne Klein, Les tactiques de Kronos

$v_{0}$

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- Etienne Klein, Les tactiques de Kronos



## Timed Domains

## Definition

A timed domain is a couple $\langle V, \hookrightarrow\rangle$ where $V$ is a set called value space and $\hookrightarrow$ is a function from $\mathbb{R}_{\geq 0}$ to $\mathcal{P}(V \times V)$ called delay transition, such that

- for all $v \in V,(v, v) \in \hookrightarrow(0)$
- for all $v \in V$ and $d \in \mathbb{R}_{\geq 0}$, there exists $v^{\prime} \in V$ such that $\left(v, v^{\prime}\right) \in \hookrightarrow(d)$
- for all $d, d^{\prime} \in \mathbb{R}_{\geq 0}$, for all $v, v^{\prime}, v^{\prime \prime} \in V$,

$$
\text { if }\left(v, v^{\prime}\right) \in \hookrightarrow(d) \text { and }\left(v^{\prime}, v^{\prime \prime}\right) \in \hookrightarrow\left(d^{\prime}\right) \text { then }\left(v, v^{\prime \prime}\right) \in \hookrightarrow\left(d+d^{\prime}\right)
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$$

Example: The $M$-bounded clock domain is

$$
\langle[0 ; M] \cup\{\infty\}, \hookrightarrow\rangle
$$

In the 5 -bounded clock domain $3 \xrightarrow{1} 4 \xrightarrow{1.2} \infty$

## Timed Structures



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## Timed Structures

## Definition

Let $D=\langle V, \hookrightarrow\rangle$ be a timed domain. An update set on $D$ is a subset of $V^{V}$.

## Definition

A timed structure is a triple $T=\langle V, \hookrightarrow, U\rangle$ where $\langle V, \hookrightarrow\rangle$ is a timed domain and $U$ is an update set on $\langle V, \hookrightarrow\rangle$.

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Example: The one-dimensional clock structure can be equipped with the two updates id and $\mathbf{0}$ to form the $M$-clock structure :

$$
\langle[0 ; M] \cup\{\infty\}, \hookrightarrow,\{\mathbf{i d}, \mathbf{0}\}\rangle
$$

## Guards

Timed Structure (TS) $\langle[0 ; 2] \cup\{\infty\}, \hookrightarrow,\{\mathbf{i d}, \mathbf{0}\}\rangle$

## Definition

Given a timed structure $\mathcal{S}=(V, \hookrightarrow, U)$ we call guard on $\mathcal{S}$ any subset of $V \times U$.

## Guards

$$
\begin{array}{ll}
\text { Timed Structure }(T S) & \langle[0 ; 2] \cup\{\infty\}, \hookrightarrow,\{\text { id }, 0\}\rangle \\
\text { Guard } & {\left[0,1\left[\times\{\mathbf{0}\} \cup\left\{\left(\frac{\pi}{2}, \text { id }\right)\right\}\right.\right.} \\
\text { TA Notations } & 0 \leq x<1 ; x:=0 \text { or } x=\frac{\pi}{2}
\end{array}
$$

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## Timed Structure (TS)

$$
\langle[0 ; 2] \cup\{\infty\}, \hookrightarrow,\{\mathrm{id}, 0\}\rangle
$$

Guard
TA Notations
Guard Basis
TA Notations

Example

## Definition

Given a timed structure $\mathcal{S}=(V, \hookrightarrow, U)$ we call guard on $\mathcal{S}$ any subset of $V \times U$.

## Guards

## Guard <br> TA Notations <br> Guard Basis <br> TA Notations <br> Example

Timed Structure (TS)

## Guarded TS

$$
\begin{aligned}
& \langle[0 ; 2] \cup\{\infty\}, \hookrightarrow,\{\mathbf{i d}, \mathbf{0}\}\rangle \\
& {\left[0,1\left[\times\{\mathbf{0}\} \cup\left\{\left(\frac{\pi}{2}, \text { id }\right)\right\}\right.\right.} \\
& 0 \leq x<1 ; x:=0 \text { or } x=\frac{\pi}{2} \\
& \mathcal{G}=\{\{0\},] 0 ; 1[,\{1\},] 1 ; 2[,\{2\},\{\infty\}\} \times\{\mathbf{0}, \text { id }\} \\
& x=0,0<x<1, x=1,1<x<2, x=2, x>2 \\
& \text { with a potential reset on } x \\
& {[1,2[\times\{\mathbf{0}, \text { id }\}=} \\
& \{(1, \mathbf{0})\} \cup] 1,2[\times\{\mathbf{0}\} \cup\{(1, \text { id })\} \cup] 1,2[\times\{\text { id }\}
\end{aligned}
$$

$$
\langle[0 ; 2] \cup\{\infty\}, \hookrightarrow,\{\mathbf{i d}, \mathbf{0}\}, \mathcal{G}\rangle
$$

## Definition

Let $\mathcal{S}=\langle V, \hookrightarrow, U\rangle$ be a timed structure and let $G$ be a guard basis on $\mathcal{S}$. The tuple $\mathcal{S}_{G}=\langle V, \hookrightarrow, U, G\rangle$, is named guarded timed structure.

## Automata on Timed Structures

## Definition

Fix $\mathcal{S}=\langle V, \hookrightarrow, U\rangle$, a timed structure. An automaton on $\mathcal{S}$ is a tuple

$$
A=\langle Q, I, T, F\rangle
$$

where $Q$ is a finite set of states, $I \subseteq Q \times V$ is the set of initial configurations, $T \subseteq Q \times V \times U \times Q$ is the transition relation, and $F \subseteq Q$ is the set of final states.
We write $\mathbb{A}(\mathcal{S})$ for the set of automata over the timed structure $\mathcal{S}$.

## Automata on Timed Structures

If $\mathcal{S}_{\mathcal{G}}$ is a guarded timed structure and the guards of an automaton $A$ are decomposable on the guard basis $\mathcal{G}$ we say that $A$ is compatible with $\mathcal{G}$ and write $A \in \mathbb{A}\left(\mathcal{S}_{\mathcal{G}}\right)$.


## Automata on Timed Structures

An automaton $A=\langle Q, I, T, F\rangle$ induces an labeled infinite-state transition system on $Q \times V$.

$$
\begin{aligned}
&(q, v) \xrightarrow{d}\left(q^{\prime}, v^{\prime}\right) \Leftrightarrow \quad q=q^{\prime} \text { and } v \stackrel{d}{\hookrightarrow} v^{\prime} \\
&(q, v) \xrightarrow{u}\left(q^{\prime}, v^{\prime}\right) \quad \Leftrightarrow \quad\left(q, v, u, q^{\prime}\right) \in T \text { and } v^{\prime}=u(v) .
\end{aligned}
$$

Example: A trace of an automaton in $\mathbb{A}(\langle[0 ; 2] \cup\{\infty\}, \hookrightarrow,\{\mathbf{i d}, \mathbf{0}\}\rangle)$.

$$
\left(q_{1}, 0\right) \xrightarrow{1.2}\left(q_{1}, 1.2\right) \xrightarrow{0}\left(q_{2}, 0\right) \xrightarrow{3}\left(q_{2}, \infty\right) \xrightarrow{\text { id }}\left(q_{3}, \infty\right)
$$

## Controls



## Full Controls

$$
[0,1] \cup\{\infty\},(\mathbf{a}, \mathbf{i d}),\{\mathbf{i d}\} \quad[0,1] \cup\{\infty\},(\mathbf{a}, \mathbf{i d}),\{\mathbf{i d}\}
$$



All runs recognizing $(a, \mathbf{i d}) \cdot(a, \mathbf{0}) \cdot 1 \cdot(a, \mathbf{i d})$ :

$$
\left(q_{1}, 0\right) \xrightarrow{(a, i d)}\left(q_{1}, 0\right) \xrightarrow{(a, 0)}\left(q_{2}, 0\right) \xrightarrow{1}\left(q_{2}, 1\right) \xrightarrow{(a, i d)}\left\{\begin{array}{l}
\left(q_{3}, 1\right) \\
\left(q_{2}, 1\right)
\end{array}\right.
$$

## Timed Controls

$$
[0,1] \cup\{\infty\}, a,\{\mathbf{i d}\} \quad[0,1] \cup\{\infty\}, a,\{\mathbf{i d}\}
$$



All runs recognizing $a \cdot a \cdot 1 \cdot a$ :

$$
\begin{aligned}
& \left(q_{2}, 0\right) \xrightarrow{a}\left(q_{2}, 0\right) \xrightarrow{1}\left(q_{2}, 1\right) \xrightarrow{a}\left\{\begin{array}{l}
\left(q_{2}, 1\right) \\
\left(q_{3}, 1\right)
\end{array}\right.
\end{aligned}
$$

## General Powerset Construction

## Theorem

Let $\Sigma$ a finite alphabet, $\mathcal{S}$ a timed structure and $A$ an automaton on $\mathcal{S}$ equipped with a timed control $\kappa$ over $\Sigma$ and without silent transitions. $A$ is $\Sigma$-determinizable ; i.e. there exists $A^{\prime}$ an automaton on $\mathbf{D}_{A, \kappa} \mathcal{S}$ equipped with a timed control $\mathbf{D} \kappa$ such that $A^{\prime}$ is deterministic w.r.t $\mathbf{D} \kappa$ and $A^{\prime}$ recognize the same language as $A$.
Moreover, if $A$ is finitely representable, we can construct a determinized automaton of $A$ with a finite representation.

## General Powerset Construction



## General Powerset Construction

$\mathrm{D} \mathcal{B}$ : $\qquad$


## Example of Powerset Construction

$$
\begin{aligned}
& \text { a, } q_{2} \cap\{1\}=\emptyset, \\
& \left.\rightarrow \begin{array}{ll}
{\left[\begin{array}{ll}
q_{1}: & x \rightarrow q_{1} \\
q_{1}: & 0
\end{array}\right] q_{2}}
\end{array}\right]
\end{aligned}
$$

## Classical Determinization

- Bounded Sets Case $\longrightarrow[\text { BBBB09 }]^{1}$
- Strongly non-Zeno Timed Automata
- 0-Bounded Timed Automata [OW04] ${ }^{2}$
- Integer Reset Timed Automata [SPKM08] ${ }^{3}$
- Finally Imprecise Timed Automata

[^0]
## Input-determined models

## Theorem

Let $\Sigma$ a finite alphabet, $\mathcal{S}_{G}$ a guarded deterministic timed structure where $U$ is finite and $A \in \mathbb{A}\left(\mathcal{S}_{G}\right)$ equipped with a compatible $\Sigma$-full control. Then $A$ can be $\Sigma$-determinized in the same guarded timed structure $\mathcal{S}_{G}$.

[^1]
## Input-determined models

## Theorem

Let $\Sigma$ a finite alphabet, $\mathcal{S}_{G}$ a guarded deterministic timed structure where $U$ is finite and $A \in \mathbb{A}\left(\mathcal{S}_{G}\right)$ equipped with a compatible $\Sigma$-full control. Then $A$ can be $\Sigma$-determinized in the same guarded timed structure $\mathcal{S}_{G}$.

## Applications.

- Event-clock automata [AFH94] ${ }^{4}$
- (Timed) Visibly Pushdown Automata [AAS] ${ }^{5}$
- Strict Integer Reset Timed Automata [BG17] ${ }^{6}$

[^2]
## Step 2

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## Toward Diagnosis



## What's left to be done

| Timed Automaton | Powerset construction |
| :---: | :---: |
| $\xrightarrow{a}$ | $\mathbf{U}_{a}$ |
| $\xrightarrow{d}$ | $\mathbf{U}_{d}$ |

## What's left to be done

| Timed Automaton | Powerset construction |  |
| :---: | :---: | :--- |
| $\xrightarrow{a}$ | $\mathbf{U}_{a}$ | easy to compute |
| $\xrightarrow{d}$ | $\mathbf{U}_{d}$ |  |

## What's left to be done

| Timed Automaton | Powerset construction |  |
| :---: | :---: | :---: |
| $\xrightarrow{a}$ | $\mathbf{U}_{a}$ | easy to compute |
| $\xrightarrow{d}$ | $\mathbf{U}_{d}$ | difficult to compute |

## What's left to be done



## Regular Timed Interval



## $\mathbf{U}_{0}$

$q_{0}:\{0\}$
$q_{1}: \quad \emptyset$

## Regular Timed Interval



|  | $\mathbf{U}_{0}$ | $\mathbf{U}_{2}$ |
| :---: | :---: | :---: |
| $q_{0}:$ | $\{0\}$ | $\{2\}$ |
| $q_{1}:$ | $\emptyset$ | $\{2\}$ |

## Regular Timed Interval



|  | $\mathbf{U}_{0}$ | $\mathbf{U}_{2}$ | $\mathbf{U}_{3.5}$ |
| :---: | :---: | :---: | :---: |
| $q_{0}:$ | $\{0\}$ | $\{2\}$ | $\{3.5\} \cup[0 ; 0.5[$ |
| $q_{1}:$ | $\emptyset$ | $\{2\}$ | $\{3.5\}$ |

## Regular Timed Interval



|  | $\mathbf{U}_{0}$ | $\mathbf{U}_{2}$ | $\mathbf{U}_{3.5}$ | $\mathbf{U}_{8}$ |
| :---: | :---: | :---: | :---: | :---: |
| $q_{0}:$ | $\{0\}$ | $\{2\}$ | $\{3.5\} \cup[0 ; 0.5[$ | $\{8\} \cup[4,5[\cup[0,2[$ |
| $q_{1}:$ | $\emptyset$ | $\{2\}$ | $\{3.5\}$ | $\{8\} \cup[4,5[\cup[1,2[$ |

## Regular Timed Interval



## Regular Timed Interval



## Regular Timed Interval



## Regular Timed Interval



## Regular Timed Interval

|  | $\mathbf{U}_{3.5}$ |
| :---: | :---: |
| $q_{0}:$ | $\{3.5\} \cup[0,0.5[$ |
| $q_{1}:$ | $\{3.5\}$ |



## Regular Timed Interval



## Regular Timed Interval



## Regular Timed Interval

|  | $\mathbf{U}_{6}$ |
| :---: | :---: |
| $q_{0}:$ | $\{6\} \cup[2,3[$ |
| $q_{1}:$ | $\{6\} \cup[2,3[$ |



## Regular Timed Interval

$\mathbf{U}_{7}$
$q_{0}:\{7\} \cup[3,4[\cup[0,1[$
$q_{1}: \quad\{7\} \cup[3,4[$


## Regular Timed Interval

$\mathbf{U}_{8}$
$q_{0}:\{8\} \cup[4,5[\cup[0,2[$

$$
q_{1}:\{8\} \cup[4,5[\cup[1,2[
$$



## Regular Timed Interval



## Regular Timed Interval

- A delay transition on the powerset automaton is equivalent to an addition on regular timed intervals once $\boldsymbol{\epsilon}$ have been applied
- The operator $\epsilon$ is computable by sequential set theoretic operations
- Most of interval part of the computation can be precomputed
- Computing a delay can be done in constant time once the $\boldsymbol{\epsilon}$ have been applied


## Step 3

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## DOTA

- $\approx 5500$ lines of Python code
- Implementation of both methods
- Library for Regular Timed Intervals
- Several ways of using the diagnoser using channels


## DOTA



## Benchmark

|  | Example2 | Example3 | Example4 | Example6 | Example8 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| \#State/\#Silent Trans | $3 / 6$ | $4 / 6$ | $4 / 7$ | $7 / 10$ | $7 / 5$ |
| Precomputation Time | 173.25 s | 0.38 s | 791.06 s | 11.01 s | 4.96 s |
| Actions DiagOTA | 0.014 s | 0.019 s | 0.029 s | 0.17 s | 0.15 s |
| Actions TripakisDOTA | 0.020 s | 0.078 s | 0.049 s | 0.26 s | 0.042 |
| Ratio (actions) | 0.73 | 0.25 | 0.59 | 0.64 | 3.71 |
| Delays Diag0TA | 0.000012 s | 0.0000011 s | 0.000011 s | 0.000011 s | 0.000012 s |
| Delays TripakisDOTA | 0.032 s | 0.057 s | 0.049 s | 0.30 s | 0.033 s |
| Ratio (delays) | 0.0004 | 0.0002 | 0.0002 | 0.00003 | 0.0004 |

Bench for 5 examples over 400 runs with 10 to 20 actions

## Conclusion

- New quantitative model : Automata on Timed Structures
- General powerset construction
- Comparison with existing work
- Exploitation of the powerset construction in the context of diagnosis
- Comparison of our diagnoser with the diagnoser constructed by Tripakis


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## Perspectives

- Improve DOTA and the benchmark
- Extend the diagnoser construction to n-clock timed automata
- Export classical theoretical result in the framework of automata on timed structures.


## Thank You




[^0]:    ${ }^{1}$ Baier, Bertrand, Bouyer, and Brihaye. When Are Timed Automata Determinizable? ICALP09
    ${ }^{2}$ Ouaknine and Worrell. On the language inclusion problem for timed automata: Closing a decidability gap. LICS04
    ${ }^{3}$ Suman, Pandya, Krishna and Manasa. Timed Automata with Integer Resets: Language Inclusion. . . FORMATS08

[^1]:    ${ }^{4}$ Alur, Fix, and Henzinger. A determinizable class of timed automata. CAV94
    ${ }^{5}$ Abdulla, Atig, and Stenman. Dense-timed pushdown automata LICS12
    ${ }^{6}$ Bhave and Guha. Adding dense-timed stack to integer reset timed automata. RP17

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