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Numerical simulation and physical experimentation of a 5-level and 7-level power converter under a control designed by a formal method

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Abstract. High-power converters based on elementary switching cells are more and more used in the industry of power electronics owing to various advantages such as lower voltage stress and reduced power loss. However, the complexity of controlling such converters is a major challenge that the power manufacturing industry has to face with. The synthesis of industrial switching controllers relies today on heuristic rules and empiric simulation. There is no formal guarantee of correctness in zones around nominal values. In [3], we have applied a backward-oriented formal method to guarantee the good behavior of the systems within predefined zones of variations for the input parameters. Here, for numerical stability reasons, we choose to use a forward-oriented method. We apply this method to a 5-level and 7-level power converters. We check the correctness of our approach by numerical simulations and physical experimentations.

1 Introduction

The general function of a multilevel power converter is to synthesize a desired voltage from several levels of dc voltage. For this reason, multilevel power converters can easily provide the high power required of a large electric drive (see [8]).
Schematically, a multilevel converter is made of n capacitors $C_1, \ldots, C_n$ and n switching cells $S_1, \ldots, S_n$ (as well as n opposite switching cells which are in complementary positions). This is schematized on Fig. 1. According to the positions of S_i (the high-side switch conducting position is indicated by 1 and the lowside switch conducting position by 0), one is able to fraction the load voltage v_0. By controlling the global position of the switches during a simple fixed time-stepping procedure, one is thus able to produce a n-level staircase output signal (see Fig. 2).
As the number n of level increases, the synthesized output has more steps, which produces a staircase wave that approaches a desired waveform. As more steps are added to the waveform, the harmonic distortion of the ouput wave decreases approaching zero. However the control problem of finding the appropriate sequence of positions for the n cells at switching

times becomes difficult because the number of combinations increases exponentially with n. Furthermore, among all the control sequences ensuring functionally the n-level staircase signal, many sequences are not acceptable because they do not satisfy the crucial requirement of *capacitor voltage balancing*: the voltage of each individual capacitor should stay inside a limited interval. In order to be acceptable, the control must ensure that the voltages across the cell-capacitors are constrained within the range defined by the device blocking voltage rating.

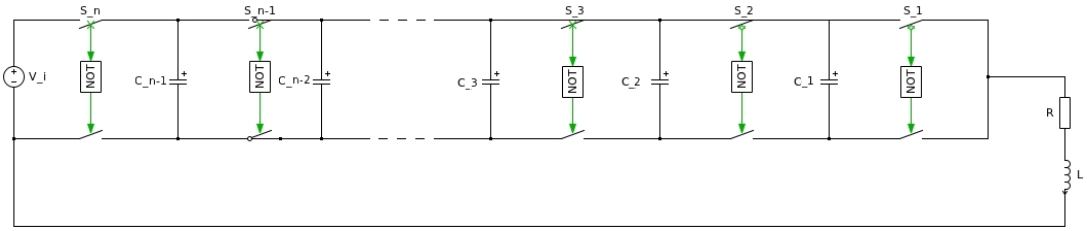


Fig. 1. Electrical scheme of an n-level converter

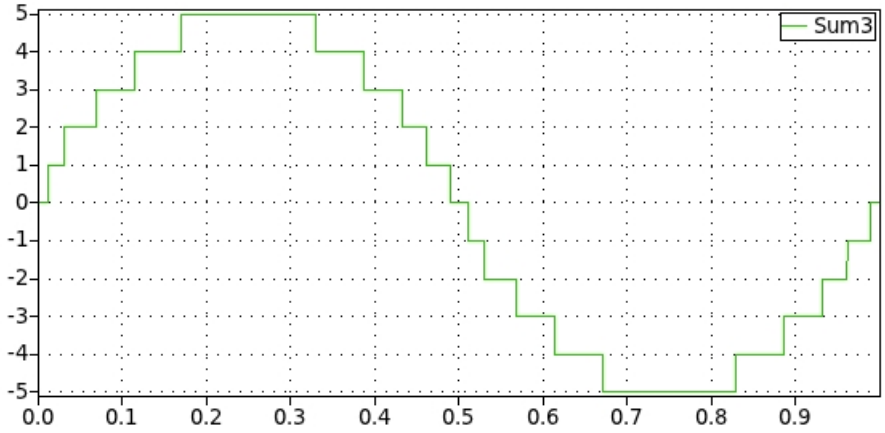


Fig. 2. Staircase output voltage waveform for a 11-level converter

In power electronics manufacturing, the synthesis of switching controllers relies today on heuristic rules and empiric criteria which are tested only for specific initial values of the voltage parameters (see, e.g., [9]). There is no formal guarantee that, during time, the system voltages will not exceed the acceptable rates. It is therefore interesting to apply formal method in order to guarantee the correct behavior of the systems for a

predefined dense set of initial values. There are different possible topologies for such an electronical device: neutral-point clamped, cascaded H-bridge, flying capacitor... (see [7]). We focus here on the flying capacitor toplogy [6]. In [3], we have applied a backward-oriented formal method to guarantee the good behavior of the systems within predefined zones of variations for the input parameters. Here, for numerical stability reasons, we choose to use a forward-oriented method. We apply this method to a 5-level and 7-level power converters. We check the correctness of our approach by numerical simulations and physical experimentations.

2 Model of sampled switched systems

In this paper, we consider a subclass of hybrid systems [5], called "switched systems" in [4].

Definition 1. *A* switched system Σ *is a quadruple* $(\mathbb{R}^n, P, \mathcal{P}, F)$ *where:*
- $\mathbb{R}^n$ *is the state space*
- $P = \{1, \ldots, m\}$ *is a finite set of* modes*,*
- $\mathcal{P}$ *is a subset of* $\mathcal{S}(\mathbb{R}_{\geq 0}, P)$ *which denotes the set of piecewise constant functions from* $\mathbb{R}_{\geq 0}$ *to* P*, continuous from the right and with a finite number of discontinuities on every bounded interval of* $\mathbb{R}_{>0}$
- $F = \{f_p \mid p \in P\}$ *is a collection of functions indexed by* P*.*

For all $p \in P$, we denote by Σ_p the continuous subsystem of Σ defined by the differential equation:

$$\dot{\mathbf{x}}(t) = f_p(\mathbf{x}(t)).$$

A *switching signal* of Σ is a function $\mathbf{p} \in \mathcal{P}$, the discontinuities of $\mathbf{p}$ are called *switching times*. A piecewise $\mathcal{C}^1$ function $\mathbf{x} : \mathbb{R}_{>0} \to \mathbb{R}^n$ is said to be a *trajectory* of Σ if it is continuous and there exists a switching signal $\mathbf{p} \in \mathcal{P}$ such that, at each $t \in \mathbb{R}_{>0}$, $\mathbf{x}$ is continuously differentiable and satisfies:

$$\dot{\mathbf{x}}(t) = f_{\mathbf{p}(t)}(\mathbf{x}(t)).$$

We will use $\mathbf{x}(t, x, \mathbf{p})$ to denote the point reached at time $t \in \mathbb{R}_{>0}$ from the initial condition x under the swiching signal $\mathbf{x}$. Let us remark that a trajectory of Σ_p is a trajectory of Σ associated with the constant signal $\mathbf{x}(t) = p$, for all $t \in \mathbb{R}_{>0}$.
In this paper, we focus on the case of *linear* switched systems: for all $p \in P$, the function f_p is defined by $f_p(x) = A_p x + b_p$ where A_p is a $(n \times n)$-matrix of constant elements $(a_{i,j})_p$ and b_p is a n-vector of constant elements $(b_k)_p$.
In the following, as in [4], we will work with trajectories of duration τ for some chosen $\tau \in \mathbb{R}_{\geq 0}$, called "time sampling parameter". This can be seen as a sampling process. Particularly, we suppose that switching instants can only occur at times of the form $i\tau$ with $i \in \mathbb{N}$. In the following, we will consider transition systems that describe trajectories of duration τ, for some given *time sampling parameter* $\tau \in \mathbb{R}_{\geq 0}$.

Definition 2. *Let* $\Sigma = (\mathbb{R}^n, P, \mathcal{P}, F)$ *be a switched system and* $\tau \in \mathbb{R}_{\geq 0}$ *a time sampling parameter. The* τ-sampled transition system associated to Σ*, denoted by* $T_\tau(\Sigma)$ *, is the transition system* $(Q, \rightarrow_\tau^p)$ *defined by:*

– *the set of states is* $Q = \mathbb{R}^n$
– *the transition relation is given by*

$$x \rightarrow_\tau^p x' \text{ iff } \mathbf{x}(\tau, x, p) = x'$$

The electrical scheme of a 5-level converter is given in (see Figure 3). The system can output 5 different levels of voltage $-1, -\frac{1}{2}, 0, \frac{1}{2}, 1$.The goal of the system is to output a staircase signal of the form presented in Figure 4.

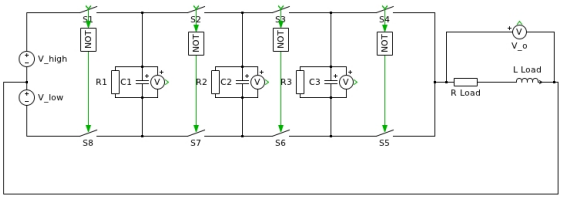


Fig. 3. Electrical scheme of the 5-level converter

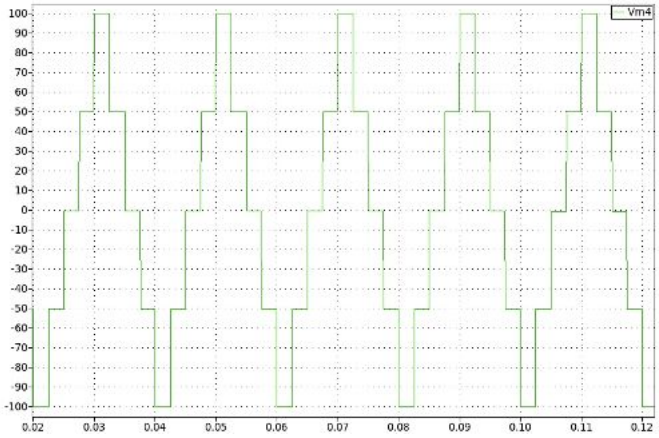


Fig. 4. Ideal output for a 5-level converter

Let v_1 (resp. v_2, v_3) be the voltage at the capacitor C_1 (resp. C_2, C_3), R_{Load} the resistor in the load, L_{Load} (abbreviated hereafter as L) the inductor in the load, v_{high} and v_{low} the input voltage. The mode of the system is characterized by the position (0 or 1) of the switching cells

S_1, S_2, S_3, S_4, i.e., by the value of vector $S = \begin{pmatrix} S_1 \\ S_2 \\ S_3 \\ S_4 \end{pmatrix}$.[1] There are thus $2^3 = 8$ modes. We will use the numerical values:

- $v_{high} = v_{low} = 100\text{V}$
- $R_{Load} = 50\Omega$
- $C_1 = C_2 = C_3 = 0.0012\text{F}$
- $L = 0.20\text{H}$
- $R_1 = R_2 = R_3 = R_4 = 20,000\Omega$

The state of the system is $x(t) = [v_1(t), v_2(t), v_3(t), i(t)]^T$ where $v_1(t)$ (resp. $v_2(t)$, $v_3(t)$) is the voltage of capacitor C_1 (resp. C_2, C_3) and $i(t)$ is the current in the circuit.

This model of 5-level converter can be seen as a switched system. Given a mode, i.e. a certain value of vector S, the associated dynamics is indeed of the form $\dot{x}(t) = A_S x(t) + b_S$, since we have:
$\dot{X} = A_S.X + b_S$ with

$$A_S = \begin{pmatrix} -\frac{1}{R_1.C_1} & 0 & 0 & \frac{S_1 - S_2}{C_1} \\ 0 & -\frac{1}{R_2.C_2} & 0 & \frac{S_2 - S_3}{C_2} \\ 0 & 0 & -\frac{1}{R_3.C_3} & \frac{S_3 - S_4}{C_3} \\ \frac{S_2 - S_1}{L} & \frac{S_3 - S_2}{L} & \frac{S_4 - S_3}{L} & -\frac{R_{Load}}{L} \end{pmatrix} \text{ and } b_S = \begin{pmatrix} 0 \\ 0 \\ 0 \\ S_1 \frac{v_{high} + v_{low}}{L} \end{pmatrix}$$

By controlling the modes at each sampling time, one can synthesize a 5-level staircase function. This is schematized by the graph depicted on Fig. 5: The nodes of the graph are labelled by the configurations of the switching cells S_1, S_2,S_3 and S_4 (mode $0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110, 1111$). Each path represents a possible sequence of control for 1 cycle, leading from voltage $-v_{low}$ (state 0000) to voltage $+v_{high}$ (state 1111) through voltages $-\frac{1}{2}.v_{low}$, 0, $\frac{1}{2}.v_{high}$ then back to voltage $-v_{low}$ (state 0000) through voltages $\frac{1}{2}.v_{high}$, 0, $\frac{1}{2}.v_{low}$. There are thus 496 possible sequences of control for generating a 5-level staircase signal on 1 cycle. These sequences of control are called *patterns*, denoted by $\text{Pattern}_1, \ldots, \text{Pattern}_{496}$.

Here, it is convenient to consider the 5-level converter, not as a τ-sampled transition system with $2^4 = 16$ modes, but, more globally, as a T-sampled transition systems where T is the duration of one cycle of the staircase signal (i.e. 8τ), and modes correspond to the 496 patterns. The control problem is now to find a strategy for deciding, at each beginning of cycle, which $Pattern_i$ ($1 \leq i \leq 496$) to apply in order to maintain all the capacitor voltages within a predefined limited zone.

We thus consider the 5-level converter as a switched system where the modes correspond to the patterns $Pattern_i$ leading to the generation of one cycle of 5-level staircase output signal.

Let us define: $Post_{\text{Pattern}}(X) = \{x' \mid x \rightarrow_T^{\text{Pattern}} x' \text{ for some } x \in X\}$, where $\rightarrow_T^{\text{Pattern}}$ means $\rightarrow_\tau^{i_1} \cdots \rightarrow_\tau^{i_8}$ with $\text{Pattern} = (i_1, \ldots, i_8)$.

A subspace $V' \subseteq V$ is said to be *V-invariant by* Pattern, if $Post_{\text{Pattern}}(V') \subseteq V$.

[1] Besides, we have: $S_5 = \neg S_1$, $S_6 = \neg S_2$, $S_7 = \neg S_3$ and $S_8 = \neg S_4$.

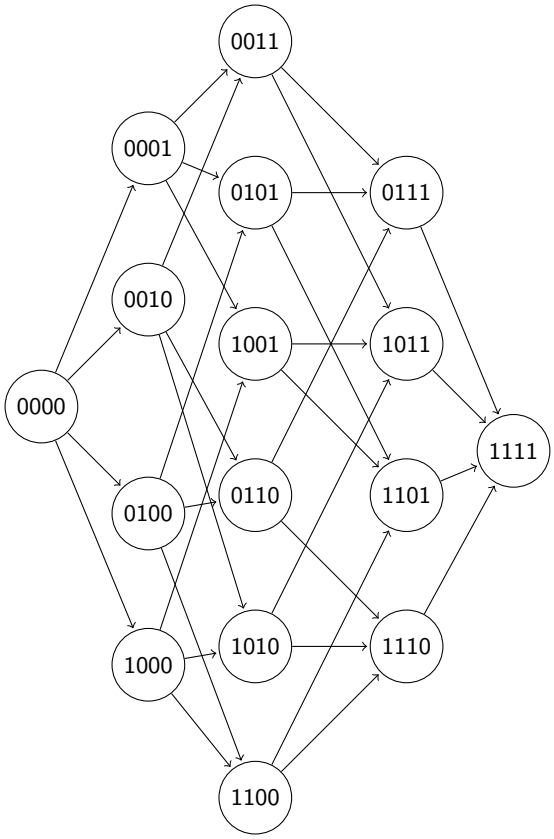


Fig. 5. Transition graph corresponding to 1/2 cycle of 5-level staircase signal

3 Forward Method of Control Synthesis

In [3], following classical work based on game theory, we have proposed a *backward* method relying on the computation of symbolic predecessors for $\rightarrow_T^{\text{Pattern}}$. Actually, since the matrices A_s have real negative eigenvalues (see Appendix A), it is more convenient for numerical stability reasons to reason in a *forward* manner and to compute symbolic successors for $\rightarrow_T^{\text{Pattern}}$. We explain this forward method on the 5-level converter. The technique applied is the following. First, we specify a box V inside which we want the system to be at every beginning of a pattern. Here, we consider V given by the following values: $V = [145, 155] \times [95, 105] \times [45, 55] \times [i_{min}, i_{max}]$, where i_{min} and i_{max} are the physical limits for i ($i_{min} = -4A$, $i_{max} = +4A$). It is interesting to notice that at each beginning of a cycle the value of i is the same. This suggests to take a state-dependent control, that takes into account only the capacitor voltages v_1, v_2, v_3 and not the value of the current intensity i. This is interesting because as noted in [2], "For practical applications, a current

sensor is not desired". We decompose V into several subset V_i such that $\bigcup_{i=1}^{8} V_i = V$. For example, let:

- $V_1 = [145, 150] \times [95, 100] \times [45, 50]$
- $V_2 = [145, 150] \times [995, 100] \times [50, 55]$
- $V_3 = [145, 150] \times [100, 105] \times [46, 50]$
- $V_4 = [145, 150] \times [100, 105] \times [50, 55]$
- $V_5 = [150, 155] \times [95, 100] \times [45, 50]$
- $V_6 = [150, 155] \times [95, 100] \times [50, 55]$
- $V_7 = [150, 155] \times [100, 105] \times [45, 50]$
- $V_8 = [150, 155] \times [100, 105] \times [50, 55]$

The basic point of the method consists in finding a pattern, say Pattern_j such that V_j is V-invariant. By convexity, we only have to find pattern Pattern_j such that every corner of V_j (including Corner_j) is V-invariant. Let Corner_j $(1 \leq j \leq 8)$ be the vertices of V. Without loss of generality, we suppose that Corner_j is a vertex of V_j. (Note that there is a one-to-one mapping between V_j and Corner_j $(1 \leq j \leq 8)$.) Using a standard random generate-and-test program, we find the following Pattern_j:

- Pattern_1: $[0000, 0001, 0101, 1101, 1111, 1101, 0101, 0001, 0000]$
- Pattern_2: $[0000, 0100, 0101, 1101, 1111, 1101, 0101, 0100, 0000]$
- Pattern_3: $[0000, 0001, 0011, 1011, 1111, 1011, 0011, 0001, 0000]$
- Pattern_4: $[0000, 0010, 0011, 1011, 1111, 1011, 0011, 0010, 0000]$
- Pattern_5: $[0000, 1000, 1010, 1110, 1111, 1110, 1010, 1000, 0000]$
- Pattern_6: $[0000, 1000, 1100, 1101, 1111, 1101, 1100, 1000, 0000]$
- Pattern_7: $[0000, 0100, 0110, 0111, 1111, 0111, 0110, 0100, 0000]$
- Pattern_8: $[0000, 1000, 1010, 1011, 1111, 1011, 1010, 1000, 0000]$

Since V_j is V-invariant by Pattern_j, we have the following control strategy:

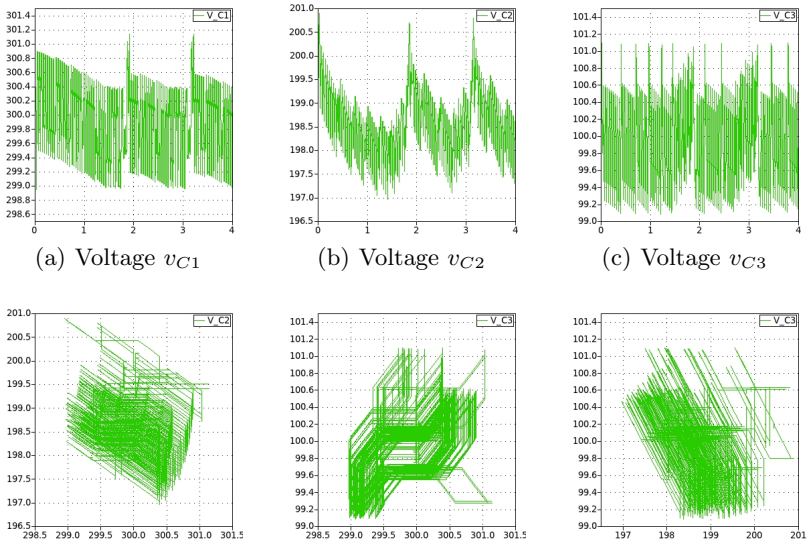
When the state of the system (v_{C1}, v_{C2}, v_{C3}) is in V_j, apply Pattern_j (when the state of the system belongs to more than one V_j, apply Pattern_j with greater j).

The result is that V is fully controllable: the system always lies within V at the beginning of each cycle. We present in Figures 6 and 7 a simulation of this controller on the system starting from the point $v_{C1}(0) = 300, v_{C2}(0) = 200, v_{C3}(0) = 100$ and $i(0) = -3$.

4 Experimentations

The 5-level flying capacitor has been realized by the SATIE Laboratory to test our control strategy on an actual system. Figure 8 is a picture of the system. Our control strategy was applied to the system via Simulink and a Dspace® card. The results are presented in Figure 9 for the output voltage and the capacitor charges. In Figure 10, we present the same results but with a larger scale on the capacitor to see the fluctuations around the reference values. As we can see, this is very close to what was obtained by the simulation with PLECS [1]. In Figure 11, we present the output voltage with the current in the circuit.

During the experimentations, we have tested the robustness of our solution to the following modifications of the system:



(a) Voltage v_{C1} (b) Voltage v_{C2} (c) Voltage v_{C3}

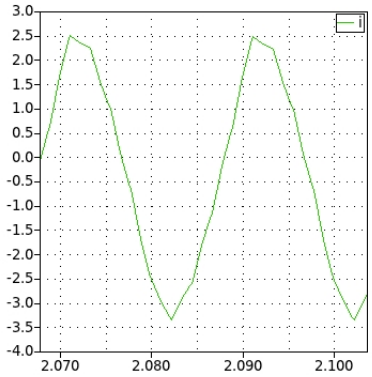
(d) Plane $v_{C2} = f(v_{C1})$ (e) Plane $v_{C3} = f(v_{C1})$ (f) Plane $v_{C3} = f(v_{C2})$

Fig. 6. Capacitor voltages

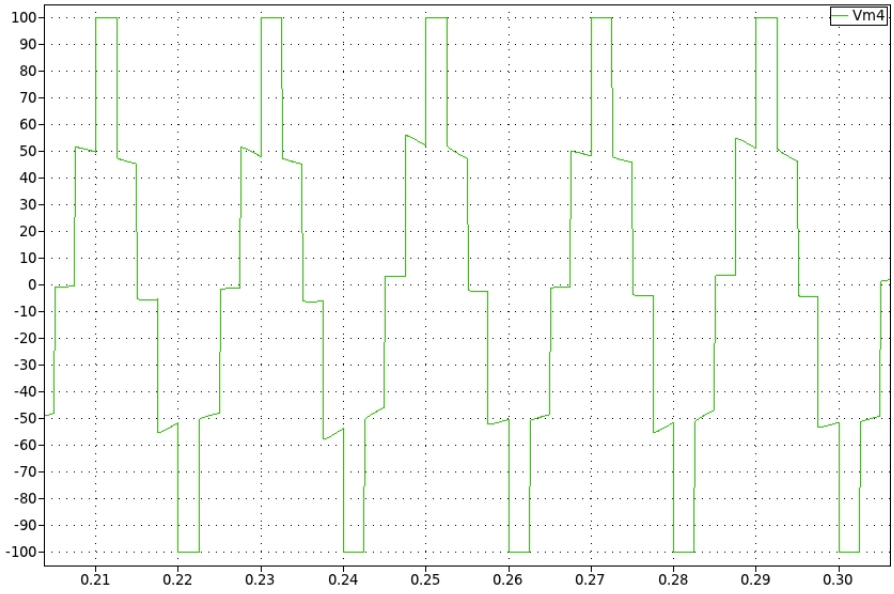
- The ideal voltage source as input is no longer ideal but its values fluctuate around the reference value.
- The system does not start from the reference valuations for the capacitor voltages and the input voltage, but the input voltage increases gradually until reaching the desired value, and the capacitor are discharged at $t = 0$.
- The switching strategy is robust to changes of the resistor load, the inductor load or both.
- We tested what happens if we apply the same pattern two times in a row instead of picking a new one at each beginning of a cycle: the system presents more fluctuations around the desired values but the capacitor voltages balancing is maintained.
- Recall that the standard strategy is to select at each T a new pattern according to the current state of the system (if the system is in V_j, one apply Pattern$_j$). Surprisingly, if we apply this strategy not periodically every T seconds (at each beginning of cycle), but following an arbitrary sequence of durations $T_1, T_2, T_3, \ldots$, the capacitor voltages remain balanced (although at some slightly different mean value). This is depicted in Figure 12. (Each vertical line is an artifact corresponding to a pattern switch.)

5 7-level Converter

In this section, we are interested in a more complex model for the converter. We will consider a 7-level converter that can generate waveform



(a) Current i



(b) Output voltage v_o

Fig. 7. Current and output voltage

going from $-v_i/2$ up to $+v_i/2$ with steps at $-v_i/2+kv_i/3$ for $k = 0, \ldots, 6$. The electrical scheme is presented in Figure 13. We used the following values for the system constants:

- Output at 50Hz
- All the capacitance equal to $0.1F$
- The resistor values 50Ω
- The inductor values $0.137H$
- $v_i = 600V$ (giving an output between $-300V$ and $+300V$)

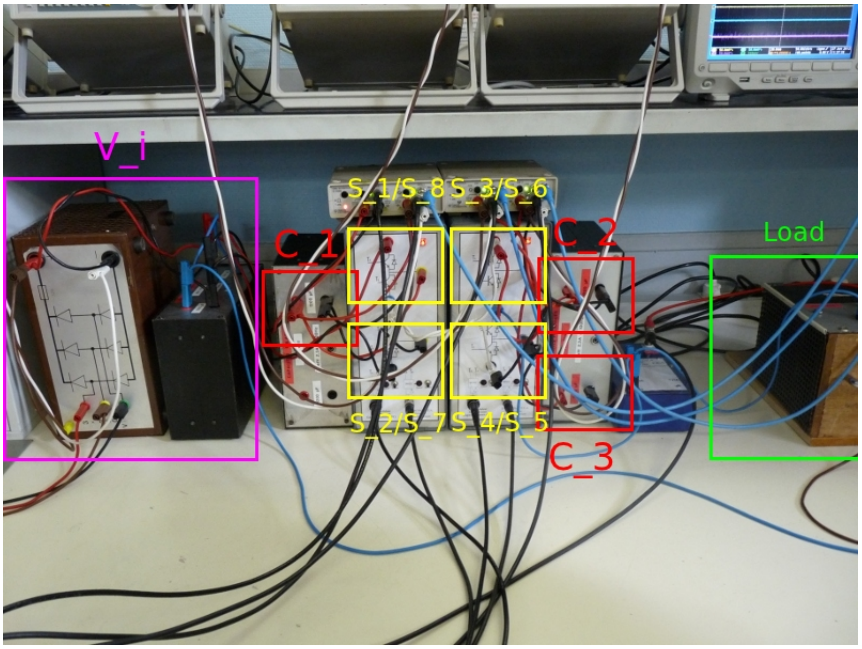


Fig. 8. Actual system build by SATIE

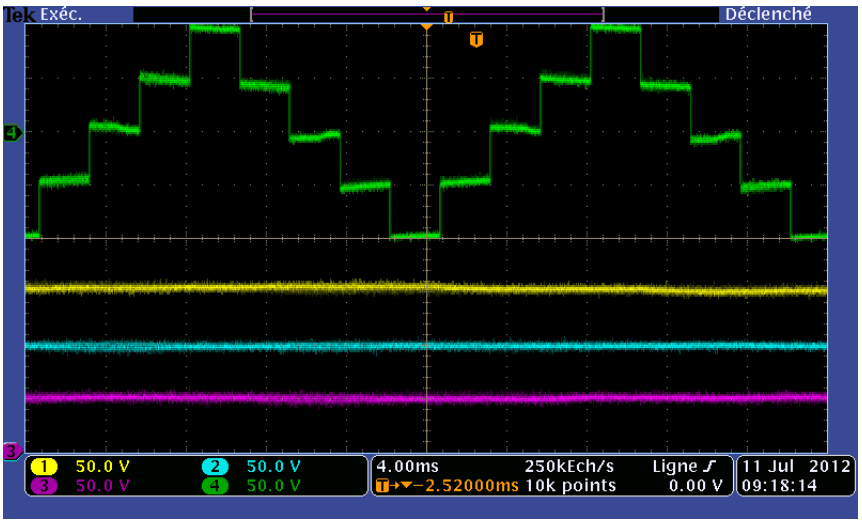


Fig. 9. Output voltage and capacitor voltages

The box V that we consider is given by the following values: $V = [596, 604] \times [496, 504] \times [396, 404] \times [296, 304] \times [196, 204] \times [96, 104] \times [i_{min}, i_{max}]$, where i_{min} and i_{max} are the physical limits for i ($i_{min} =$

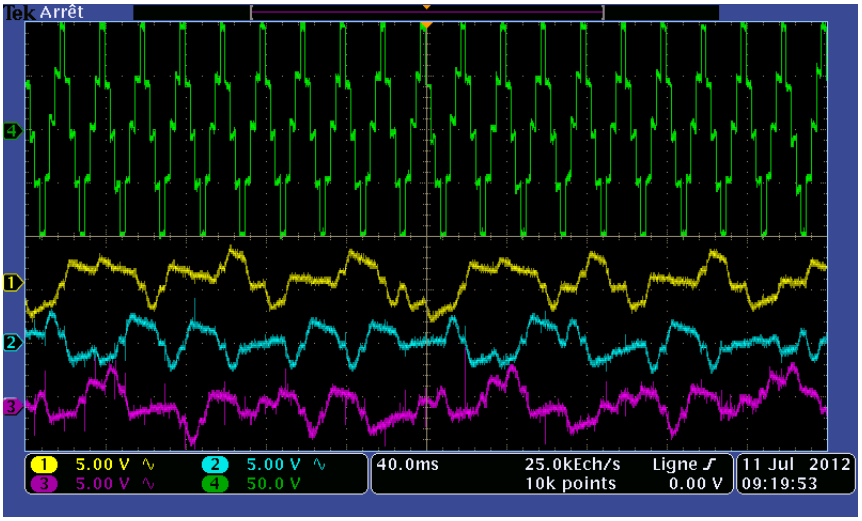


Fig. 10. Zoom of output and capacitors voltages

Fig. 11. Output voltage and current (after appropriate resizing) in the circuit

$-5A$, $i_{max} = +5A$). We observe that the pattern selection is independent from the value of i, it can be seen that we do not need to take into account the value of i for guarding the application of a specific control pattern: The guards for applying the patterns depend only on the values of v_{C1}, v_{C2}, v_{C3}, v_{C4} and v_{C5}. Let $(\text{Corner}_j)_{j\in\{1,\cdots,32\}}$ be the vertices of box V with:

– Corner_1: $(496, 396, 296, 196, 96)$

Fig. 12. Output voltage and capacitor voltages

- Corner_2: $(496, 396, 296, 196, 104)$
- Corner_3: $(496, 396, 296, 204, 96)$
- Corner_4: $(496, 396, 296, 204, 104)$
- Corner_5: $(496, 396, 304, 196, 96)$
- Corner_6: $(496, 396, 304, 196, 104)$
- Corner_7: $(496, 396, 304, 204, 96)$
- Corner_8: $(496, 396, 304, 204, 104)$
- Corner_9: $(496, 404, 296, 196, 96)$
- Corner_{10}: $(496, 404, 296, 196, 104)$
- Corner_{11}: $(496, 404, 296, 204, 96)$
- Corner_{12}: $(496, 404, 296, 204, 104)$
- Corner_{13}: $(496, 404, 304, 196, 96)$
- Corner_{14}: $(496, 404, 304, 196, 104)$
- Corner_{15}: $(496, 404, 304, 204, 96)$
- Corner_{16}: $(496, 404, 304, 204, 104)$
- Corner_{17}: $(504, 396, 296, 196, 96)$
- Corner_{18}: $(504, 396, 296, 196, 104)$
- Corner_{19}: $(504, 396, 296, 204, 96)$
- Corner_{20}: $(504, 396, 296, 204, 104)$
- Corner_{21}: $(504, 396, 304, 196, 96)$
- Corner_{22}: $(504, 396, 304, 196, 104)$
- Corner_{23}: $(504, 396, 304, 204, 96)$
- Corner_{24}: $(504, 396, 304, 204, 104)$
- Corner_{25}: $(504, 404, 296, 196, 96)$
- Corner_{26}: $(504, 404, 296, 196, 104)$
- Corner_{27}: $(504, 404, 296, 204, 96)$
- Corner_{28}: $(504, 404, 296, 204, 104)$
- Corner_{29}: $(504, 404, 304, 196, 96)$

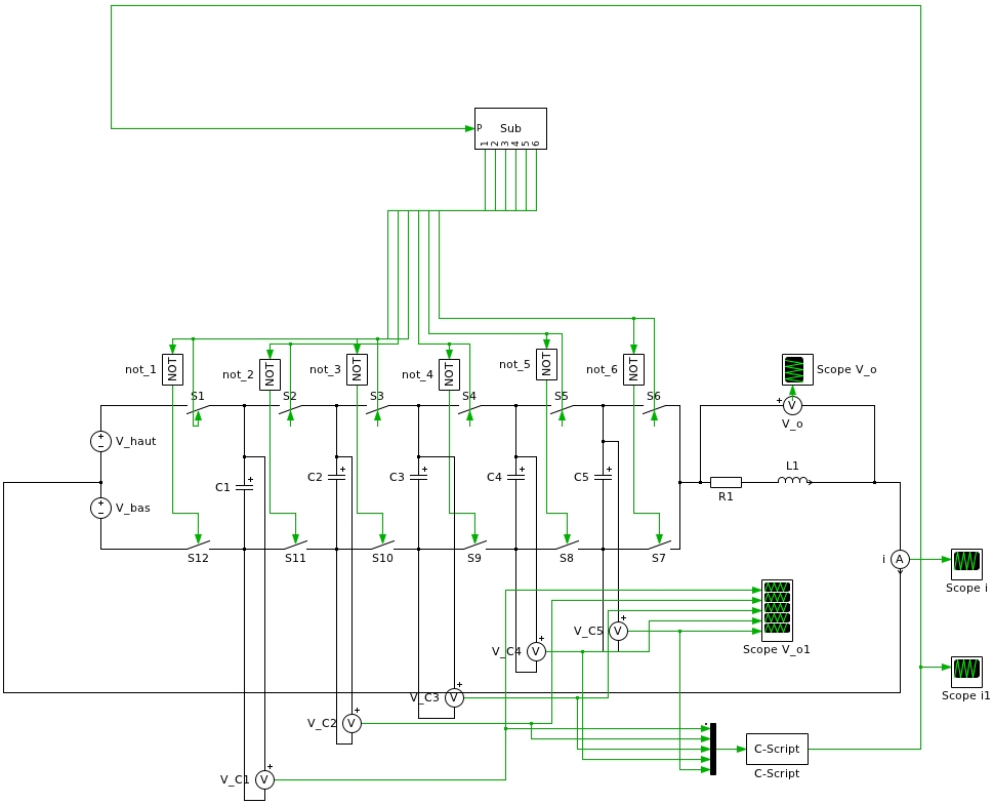


Fig. 13. Electrical scheme of the 7-level converter

– Corner_{30}: $(504, 404, 304, 196, 104)$
– Corner_{31}: $(504, 404, 304, 204, 96)$
– Corner_{32}: $(504, 404, 304, 204, 104)$.

The set $\{\text{Corner}_j\}_{1 \leq j \leq 32}$ naturally induces a dichotomous partition of V into a set of subspaces $\{V_j\}_{1 \leq j \leq 32}$. Our random generate-and-test program finds the following patterns:

– Pattern_1: $[000000, 000001, 000101, 010101, 110101, 111101, 111111, 111101, 110101, 010100, 000101, 000001, 000000]$
– Pattern_2: $[000000, 000010, 000110, 010110, 110110, 111110, 111111, 111110, 110110, 010110, 000110, 000010, 000000]$
– Pattern_3: $[000000, 000001, 001001, 011001, 111001, 111011, 111111, 111011, 111001, 011001, 001001, 000001, 000000]$
– Pattern_4: $[000000, 000010, 001010, 011010, 111010, 111011, 111111, 111011, 111010, 011010, 001010, 000010, 000000]$
– Pattern_5: $[000000, 001000, 011000, 111000, 111100, 111110, 111111, 111110, 111100, 111000, 011000, 001000, 000000]$
– Pattern_6: $[000000, 001000, 011000, 111000, 111001, 111101, 111111, 111101, 111001, 111000, 011000, 001000, 000000]$

- Pattern_{7}: [000000, 001000, 011000, 111000, 111010, 111011, 111111, 111011, 111010, 111000, 011000, 001000, 000000]
- Pattern_{8}: [000000, 001000, 011000, 111000, 111001, 111011, 111111, 111011, 111001, 111000, 011000, 001000, 000000]
- Pattern_{9}: [000000, 000001, 000011, 000111, 001111, 101111, 111111, 101111, 001111, 000111, 000011, 000001, 000000]
- Pattern_{10}: [000000, 000010, 000011, 000111, 001111, 101111, 111111, 101111, 001111, 000111, 000011, 000010, 000000]
- Pattern_{11}: [000000, 000001, 000101, 000111, 001111, 101111, 111111, 101111, 001111, 000111, 000101, 000001, 000000]
- Pattern_{12}: [000000, 000100, 000110, 000111, 001111, 101111, 111111, 101111, 001111, 000111, 000110, 000100, 000000]
- Pattern_{13}: [000000, 000001, 000011, 001011, 001111, 101111, 111111, 101111, 001111, 001011, 000011, 000001, 000000]
- Pattern_{14}: [000000, 000010, 000011, 001011, 001111, 101111, 111111, 101111, 001111, 001011, 000011, 000010, 000000]
- Pattern_{15}: [000000, 100000, 110000, 111000, 111100, 111110, 111111, 101111, 100111, 100011, 100001, 100000, 000000]
- Pattern_{16}: [000000, 100000, 110000, 111000, 111100, 111110, 111111, 101111, 100111, 100011, 100001, 100000, 000000]
- Pattern_{17}: [000000, 000001, 000011, 000111, 001111, 011111, 111111, 111110, 111100, 111000, 110000, 100000, 000000]
- Pattern_{18}: [000000, 000010, 000110, 001110, 011110, 111111, 111111, 111110, 011110, 001110, 000110, 000010, 000000]
- Pattern_{19}: [000000, 000100, 001100, 001101, 001111, 011111, 111111, 011111, 001111, 001101, 001100, 000100, 000000]
- Pattern_{20}: [000000, 000100, 001100, 001110, 001111, 011111, 111111, 011111, 001111, 001110, 001100, 000100, 000000]
- Pattern_{21}: [000000, 000001, 001001, 001011, 001111, 011111, 111111, 011111, 001111, 001011, 001001, 000001, 000000]
- Pattern_{22}: [000000, 000010, 001010, 001011, 001111, 011111, 111111, 011111, 001111, 001011, 001010, 000010, 000000]
- Pattern_{23}: [000000, 000001, 001001, 001101, 001111, 011111, 111111, 011111, 001111, 001101, 001001, 000001, 000000]
- Pattern_{24}: [000000, 001000, 001100, 001110, 001111, 011111, 111111, 011111, 001111, 001110, 001100, 001000, 000000]
- Pattern_{25}: [000000, 000001, 000011, 000111, 001111, 011111, 111111, 011111, 001111, 000111, 000011, 000001, 000000]
- Pattern_{26}: [000000, 000010, 000011, 000111, 001111, 011111, 111111, 011111, 001111, 000111, 000011, 000010, 000000]
- Pattern_{27}: [000000, 000001, 000101, 000111, 001111, 011111, 111111, 011111, 001111, 000111, 000101, 000001, 000000]
- Pattern_{28}: [000000, 000100, 000110, 000111, 001111, 011111, 111111, 011111, 001111, 000111, 000110, 000100, 000000]
- Pattern_{29}: [000000, 000001, 000011, 001011, 001111, 011111, 111111, 011111, 001111, 001011, 000011, 000001, 000000]
- Pattern_{30}: [000000, 000010, 000011, 001011, 001111, 011111, 111111, 011111, 001111, 001011, 000011, 000010, 000000]
- Pattern_{31}: [000000, 100000, 101000, 101001, 101011, 101111, 111111, 101111, 101011, 101001, 101000, 100000, 000000]

– Pattern_{32}: $[000000, 100000, 101000, 101010, 101011, 101111, 111111, 101111, 101011, 101010, 101000, 100000, 000000]$

Since V_j is V-invariant by Pattern_j, we have the following control strategy:

When the state of the system $(v_{C1}, v_{C2}, v_{C3}, v_{C4}, v_{C5})$ is in V_j, apply Pattern_j (when the state of the system belongs to more than one V_j, apply Pattern_j with greater j).

We present in Figures 14 and 15 a simulation of this controller on the system starting from the point $v_{C1}(0) = 500, v_{C2}(0) = 400, v_{C3}(0) = 300, v_{C4}(0) = 200, v_{C5}(0) = 100$ and $i(0) = -2.5A$.

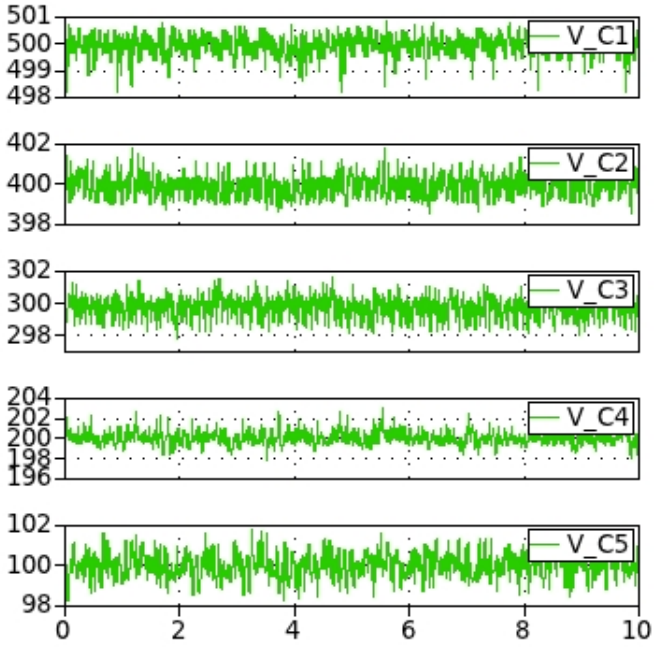
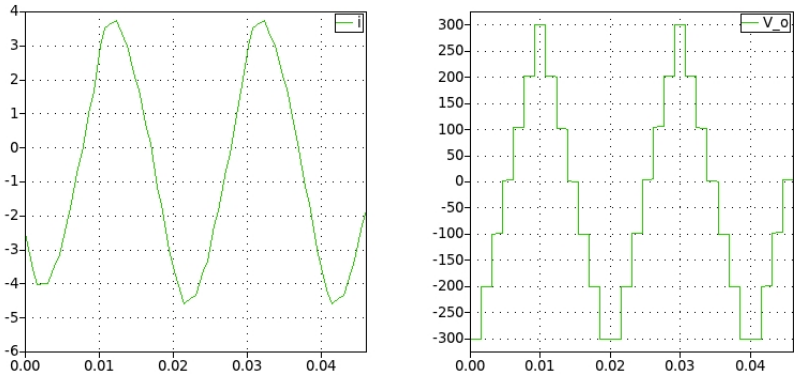


Fig. 14. Capacitor voltages

Conclusion

We have designed a control strategy for n-level ($n = 5,\ 7$) power converters using a forward-based formal method. This control is state-dependent and is interesting because:

– at each control time, the controller indicates the $2(n-1)$ subsequent switching modes (instead of just the next switching mode),
– the controller takes into account only the capacitor voltages state and not the intensity state.



(a) Current i (b) Current v_o

Fig. 15. Current and output voltage

We have checked by numerical simulations and physical experimentations that the control satisfies the capacitor voltage balancing and the staircase shape of the output voltage. We have checked the robustness of the method with respect to several sources of perturbation. The method is general and can be applied to any n-level converter, with n bigger than 7. We have observed that when a pattern lets the vertex Corner_j of V_j V-invariant, then the whole V_j is V-invariant. This can be explained intuitively by continuity and differentiability reasons. In such a case, it suffices to find patterns that let V-invariant the 2^n vertices of the global zone V. In future work, we plan to formally find conditions under which this property holds. We also plan to test the robustness of our control strategy, under variations of the resistive and inductive load (in a more systematic fashion than done here in these preliminary experiments).

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A Computation of the eigenvalues of the matrices A_S

The system is governed by the following systems: $\dot{X} = A_S.X + b_S$ with

$$A_S = \begin{pmatrix} -\frac{1}{R_1.C_1} & 0 & 0 & \frac{S_1-S_2}{C_1} \\ 0 & -\frac{1}{R_2.C_2} & 0 & \frac{S_2-S_3}{C_2} \\ 0 & 0 & -\frac{1}{R_3.C_3} & \frac{S_3-S_4}{C_3} \\ \frac{S_2-S_1}{L} & \frac{S_3-S_2}{L} & \frac{S_4-S_3}{L} & -\frac{R_{Load}}{L} \end{pmatrix} \text{ and } b_S = \begin{pmatrix} 0 \\ 0 \\ 0 \\ S_1 \frac{v_{high}+v_{low}}{L} \end{pmatrix}$$

We take the following assumptions, $R_1 = R_2 = R_3 = R$ and $C_1, C_2, C_3 = C$.
Under these assumptions it is easy to see that $-\frac{1}{R.C}$ is an eigen value or order $n-2$ or $n-1$, if $S = 0_{\mathbb{R}^n}$ or $S = 1, \ldots, 1$. The other(s) eigenvalues are $\lambda_1 = -\frac{L+CRR_{Load}+\sqrt{(L+CRR_{Load})^2-4CLR_{Load}(Ra^2+Rb^2+Rc^2+R_{Load})}}{2CLR}$ and $\lambda_2 = -\frac{L+CRR_{Load}-\sqrt{(L+CRR_{Load})^2-4CLR_{Load}(Ra^2+Rb^2+Rc^2+R_{Load})}}{2CLR}$, where $a = S_1 - S_2$, $b = S_2 - S_3$ and $c = S_3 - S_4$. It is clear that all the eigenvalues are negative.