Control of Multilevel Power Converters using Formal Methods

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Laboratoire Spécification & Vérification

École Normale Supérieure de Cachan
61, avenue du Président Wilson
94235 Cachan Cedex France

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G. Feld [2], L. Fribourg [1], D. Labrousse [2], S. Lefebvre [2], B. Revol [2] and R. Soulat [1]

[1] LSV - ENS Cachan & CNRS
[2] SATIE - ENS Cachan & CNRS

Abstract. High-power converters based on elementary switching cells are more and more used in the industry of power electronics owing to various advantages such as lower voltage stress and reduced power loss. However, the complexity of controlling such converters is a major challenge that the power manufacturing industry has to face with. The synthesis of industrial switching controllers relies today on heuristic rules and empiric simulation. There is no formal guarantee of correctness in zones around nominal values. It is therefore interesting to apply formal methods to guarantee the good behavior of the systems within predefined zones of variations for the input parameters. As far as we know, such formal methods have been applied only to small electronic power devices (like DC-DC boost converters) containing one switching cell. We show in this paper that one can apply formal methods to more complicated systems, such as multi-level converters containing several pairs of switching cells.

1 Introduction

The general function of a multilevel power converter is to synthesize a desired voltage from several levels of dc voltage. For this reason, multilevel power converters can easily provide the high power required of a large electric drive (see [12]).
Schematically, a multilevel converter is made of n capacitors $C_1, \ldots, C_n$ and n switching cells $S_1, \ldots, S_n$ (as well as n opposite switching cells which are in complementary positions). This is schematized on Fig. 1. According to the positions of S_i (the high-side switch conducting position is indicated by 1 and the lowside switch conducting position by 0), one is able to fraction the load voltage v_0. By controlling the global position of the switches during a simple fixed time-stepping procedure, one is thus able to produce a n-level staircase output signal (see Fig. 2).
As the number n of level increases, the synthesized output has more steps, which produces a staircase wave that approaches a desired waveform. As more steps are added to the waveform, the harmonic distortion of the ouput wave decreases approaching zero. However the control problem of finding the appropriate sequence of positions for the n cells at switching times becomes difficult because the number of combinations increases

exponentially with n. Furthermore, among all the control sequences ensuring functionally the n-level staircase signal, many sequences are not acceptable because they do not satisfy the crucial requirement of *capacitor voltage balancing*: the voltage of each individual capacitor should stay inside a limited interval. In order to be acceptable, the control must ensure that the voltages across the cell-capacitors are constrained within the range defined by the device blocking voltage rating.

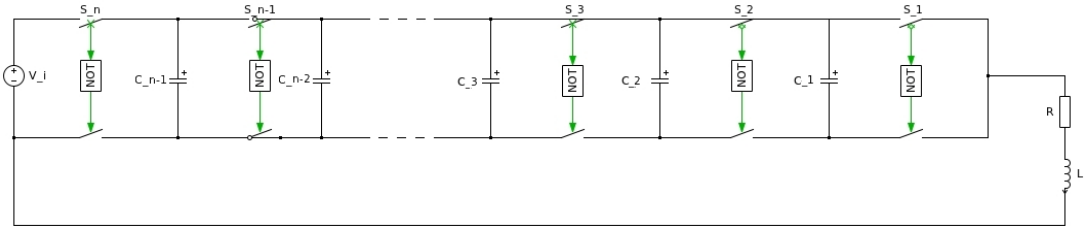

Fig. 1. Electrical scheme of an n-level converter

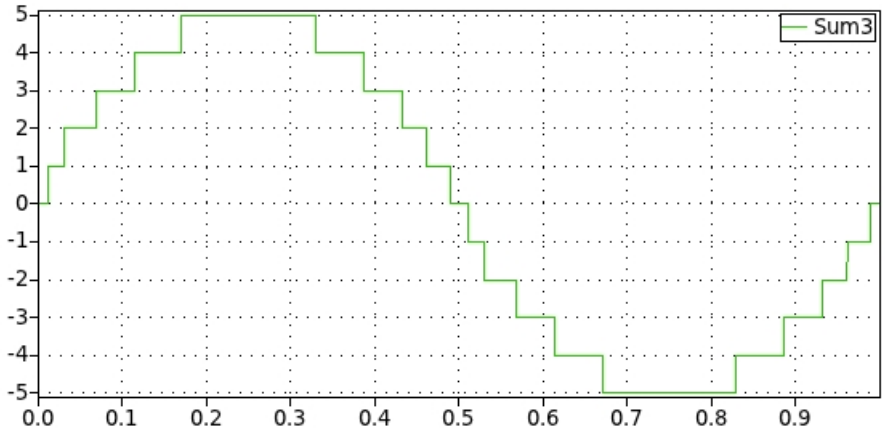

Fig. 2. Staircase output voltage waveform for a 11-level converter

In power electronics manufacturing, the synthesis of switching controllers relies today on heuristic rules and empiric criteria which are tested only for specific initial values of the voltage parameters (see, e.g., [13]). There is no formal guarantee that, during time, the system voltages will not exceed the acceptable rates. It is therefore interesting to apply formal method in order to guarantee the correct behavior of the systems for a predefined dense set of initial values. As far as we know, such formal

methods have been applied today only to small electronic power devices like boost DC-DC converters with one switching cell (see, e.g., [7, 3, 5, 10]). We show in this paper that formal methods can be successfully applied to the more complex class of multi-level converters.

Plan of the paper. In Section 2, we define the model of sampled switched systems that we use for describing multi-level converters, and the principles of our controllability method. In Section 3, we apply the method to several examples of multi-level converters. We conclude in Section 4.

2 Method of Controllability

2.1 Model of sampled switched systems

In this paper, we consider a subclass of hybrid systems [8], called "switched systems" in [7].

Definition 1. *A* switched system Σ *is a quadruple* $(\mathbb{R}^n, P, \mathcal{P}, F)$ *where:*
- $\mathbb{R}^n$ *is the state space*
- $P = \{1, \ldots, m\}$ *is a finite set of* modes*,*
- $\mathcal{P}$ *is a subset of* $\mathcal{S}(\mathbb{R}_{\geq 0}, P)$ *which denotes the set of piecewise constant functions from* $\mathbb{R}_{\geq 0}$ *to* P*, continuous from the right and with a finite number of discontinuities on every bounded interval of* $\mathbb{R}_{>0}$
- $F = \{f_p \mid p \in P\}$ *is a collection of functions indexed by* P*.*

For all $p \in P$, we denote by Σ_p the continuous subsystem of Σ defined by the differential equation:

$$\dot{\mathbf{x}}(t) = f_p(\mathbf{x}(t)).$$

A *switching signal* of Σ is a function $\mathbf{p} \in \mathcal{P}$, the discontinuities of $\mathbf{p}$ are called *switching times*. A piecewise $\mathcal{C}^1$ function $\mathbf{x} : \mathbb{R}_{>0} \to \mathbb{R}^n$ is said to be a *trajectory* of Σ if it is continuous and there exists a switching signal $\mathbf{p} \in \mathcal{P}$ such that, at each $t \in \mathbb{R}_{>0}$, $\mathbf{x}$ is continuously differentiable and satisfies:

$$\dot{\mathbf{x}}(t) = f_{\mathbf{p}(t)}(\mathbf{x}(t)).$$

We will use $\mathbf{x}(t, x, \mathbf{p})$ to denote the point reached at time $t \in \mathbb{R}_{>0}$ from the initial condition x under the swiching signal $\mathbf{x}$. Let us remark that a trajectory of Σ_p is a trajectory of Σ associated with the constant signal $\mathbf{x}(t) = p$, for all $t \in \mathbb{R}_{>0}$.

In this paper, we focus on the case of *linear* switched systems: for all $p \in P$, the function f_p is defined by $f_p(x) = A_p x + b_p$ where A_p is a $(n \times n)$-matrix of constant elements $(a_{i,j})_p$ and b_p is a n-vector of constant elements $(b_k)_p$.

In the following, as in [7], we will work with trajectories of duration τ for some chosen $\tau \in \mathbb{R}_{\geq 0}$, called "time sampling parameter". This can be seen as a sampling process. Particularly, we suppose that switching instants can only occur at times of the form $i\tau$ with $i \in \mathbb{N}$. In the following, we will consider transition systems that describe trajectories of duration τ, for some given *time sampling parameter* $\tau \in \mathbb{R}_{\geq 0}$.

Definition 2. *Let $\Sigma = (\mathbb{R}^n, P, \mathcal{P}, F)$ be a switched system and $\tau \in \mathbb{R}_{\geq 0}$ a time sampling parameter. The* τ-sampled transition system associated to Σ, *denoted by $T_\tau(\Sigma)$, is the transition system $(Q, \rightarrow_\tau^p)$ defined by:*

- *the set of states is $Q = \mathbb{R}^n$*
- *the transition relation is given by*

$$x \rightarrow_\tau^p x' \text{ iff } \mathbf{x}(\tau, x, p) = x'$$

Let us define: $Post_i(X) = \{x' \mid x \rightarrow_\tau^i x' \text{ for some } x \in X\}$, and $Pre_i(X) = \{x' \mid x' \rightarrow_\tau^i x \text{ for some } x \in X\}$.

Example 1. This example is a converter with 3 levels (see Figure 3). The system can output 3 different levels of voltage $0, \frac{1}{2}, 1$.The goal of the system is to output a staircase signal of the form presented in Figure 4.

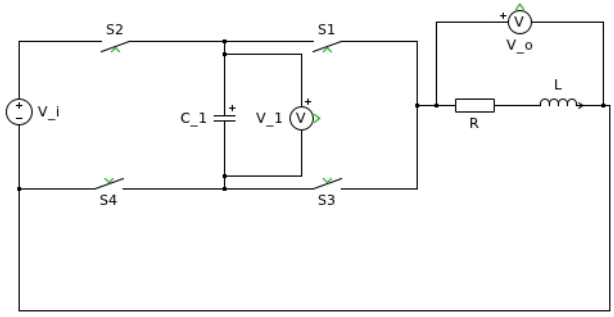

Fig. 3. Electrical scheme of the 3-level converter

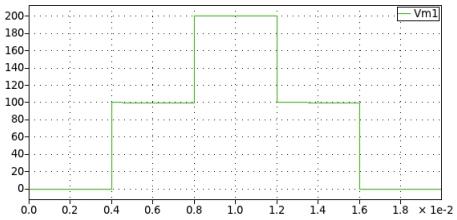

Fig. 4. Ideal output for a 3-level converter

Let v_1 be the voltage at the capacitor C_1, R the resistor in the load, L the inductor in the load, v_i the input voltage. The mode of the system is characterized by the position (0 or 1) of the switching cells S_1 and S_2, i.e., by the value of vector $S = \begin{pmatrix} S_1 \\ S_2 \end{pmatrix}$.[1] There are thus four modes: $00, 01, 10, 11$. We will use the numerical values:

[1] Besides, we have: $S_3 = \neg S_1$ and $S_4 = \neg S_2$.

– $v_i = 200\text{V}$
– $C_1 = 0.1\text{F}$
– $R = 5\Omega$
– $L = 0.0137\text{H}$

The state of the system is $x(t) = [v_1(t), i(t)]^T$ where $v_1(t)$ is the capacitor voltage and $i(t)$ is the inductor current. This model of 3-level converter can be seen as a switched system. Given a mode, i.e. a certain value of vector S, the associated dynamics is indeed of the form $\dot{x}(t) = A_S x(t) + b_S$, since we have:

$$\frac{dv_1}{dt} = S^T \times \begin{pmatrix} 1 \\ -1 \end{pmatrix} \times \frac{i}{C_1}$$

$$\frac{di}{dt} = \frac{1}{L}(S^T \times \begin{pmatrix} v_i - v_1 \\ v_1 \end{pmatrix} - R \times i)$$

By controlling the modes at each sampling time, one can synthesize a 3-level staircase function. This is schematized by the graph depicted on Fig. 5: The nodes of the graph are labelled by the configurations of the switching cells S_1 and S_2 (mode $00, 01, 10$ or 11). Each path represents a possible sequence of control for 1 cycle, leading from voltage 0 to voltage 1 through voltage $\frac{1}{2}$ then back to voltage 0 through voltage $\frac{1}{2}$. There are thus 4 possible sequences of control (called "patterns") for generating a 3-level staircase signal on 1 cycle. These patterns correspond to the paths of the graph, and denoted by:

– $Pattern_1$ for path $00 \to 01 \to 11 \to 10 \to 00$
– $Pattern_2$ for path $00 \to 10 \to 11 \to 01 \to 00$
– $Pattern_3$ for path $00 \to 01 \to 11 \to 01 \to 00$
– $Pattern_4$ for path $00 \to 10 \to 11 \to 10 \to 00$

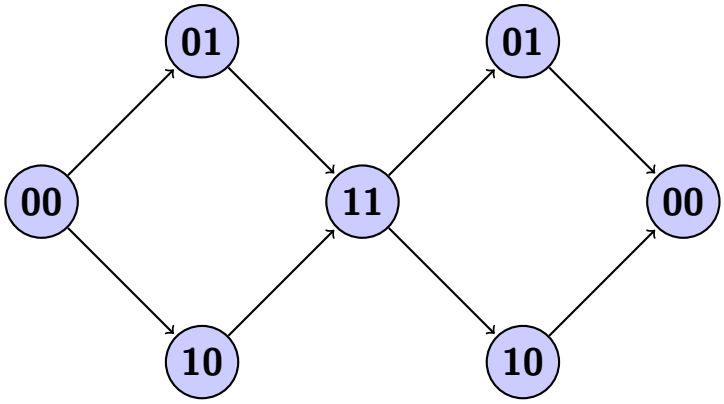

Fig. 5. Transition graph corresponding to 1 cycle of 3-level staircase signal

It is convenient to consider the 3-level converter, not as a τ-sampled transition system with modes $00, 01, 10$ and 11, but rather as a T-sampled

transition systems where T is the duration of one cycle of the staircase signal (i.e. 4τ), and modes are $Pattern_1, Pattern_2, Pattern_3$ and $Pattern_4$. The control problem is now to find a strategy for deciding, at each beginning of cycle, which $Pattern_i$ $(1 \leq i \leq 4)$ to apply in order to maintain the capacitor voltage v within a predefined limited zone.

Example 2. This example is a converter with 4 levels (see Figure 6). The system can output 4 different levels of voltage $-1, -\frac{1}{3}, \frac{1}{3}, 1$.The goal of the system is to output a staircase signal of the form presented in Figure 7.

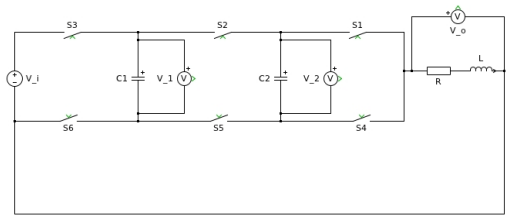

Fig. 6. Electrical scheme of the 4-level converter

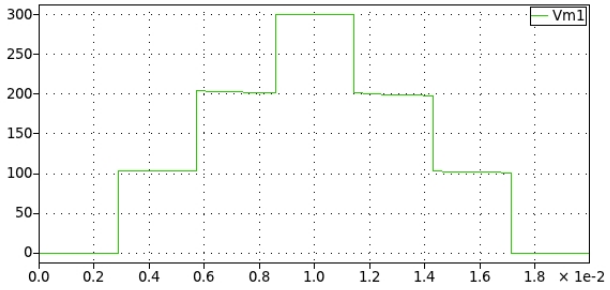

Fig. 7. Ideal output for a 4-level converter

Let v_1 (resp. v_2) be the voltage at the capacitor C_1 (resp. C_2), R the resistor in the load, L the inductor in the load, v_i the input voltage. The mode of the system is characterized by the position (0 or 1) of the switching cells S_1, S_2, S_3, i.e., by the value of vector $S = \begin{pmatrix} S_1 \\ S_2 \\ S_3 \end{pmatrix}$.[2] There are thus $2^3 = 8$ modes. We will use the numerical values:

- $v_i = 300$V

[2] Besides, we have: $S_4 = \neg S_1$, $S_5 = \neg S_2$ and $S_6 = \neg S_3$.

– $R = 5\Omega$
– $C_1 = C_2 = 0.1$F
– $L = 0.0137$H

The state of the system is $x(t) = [v_1(t), v_2(t), i(t)]^T$ where $v_1(t)$ (resp. $v_2(t)$) is the voltage of capacitor C_1 (resp. C_2) and $i(t)$ is the inductor current. It is clear that this model of 4-level converter is a switched system. Given a mode, i.e. a certain value of vector S, the associated dynamics is given by:

$$\frac{dv_1}{dt} = \frac{1}{C_1} \times S^T . \begin{pmatrix} 1 \\ -1 \\ 0 \end{pmatrix} \times i$$

$$\frac{dv_2}{dt} = \frac{1}{C_2} \times S^T . \begin{pmatrix} 0 \\ 1 \\ -1 \end{pmatrix} \times i$$

$$\frac{di}{dt} = \frac{1}{L}(S^T . \begin{pmatrix} v_i - v_1 \\ v_1 - v_2 \\ v_2 \end{pmatrix} - R \times i)$$

By controlling the modes at each sampling time, one can synthesize a 4-level staircase function. This is schematized by the graph depicted on Fig. 8: The nodes of the graph are labelled by the configurations of the switching cells S_1, S_2 and S_3 (mode $000, 001, 010, 011, 100, 101, 110, 111$). Each path represents a possible sequence of control for 1 cycle, leading from voltage 0 to voltage 1 through voltages $\frac{1}{3}$ and $\frac{2}{3}$ then back to voltage 0 through voltages $\frac{2}{3}$ and $\frac{1}{3}$. There are thus 36 possible sequences of control for generating a 4-level staircase signal on 1 cycle. Here again, it is convenient to consider the 4-level converter, not as a τ-sampled transition system with $2^3 = 8$ modes, but, more globally, as a T-sampled transition systems where T is the duration of one cycle of the staircase signal (i.e. 5τ), and modes correspond to the 36 patterns. The control problem is now to find a strategy for deciding, at each beginning of cycle, which $Pattern_i$ ($1 \leq i \leq 48$) to apply in order to maintain all the capacitor voltages within a predefined limited zone.

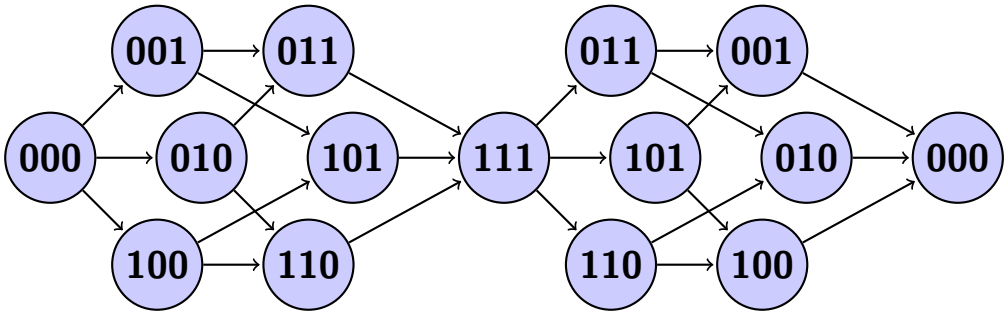

Fig. 8. Transition graph corresponding to 1 cycle of 4-level staircase signal

2.2 Principle of the method

The method that we present belongs to the *direct* approach (see [2]): it works directly on the continuous state space; it makes use of a predefined input zone V, and infers, when it terminates a *controllable* subspace V' of V: it is guaranteed that, within V', there exists a switching rule allowing to stay forever within V' (see, e.g., [11, 9]). The specific method that we use here is taken from [6]; it exploits the simple features of the subclass of systems that we consider (and which contains the model of n-level converters): linearity, absence of perturbation u, periodicity of the switching instants. The simplicity of the method comes also from the fact that we guarantee only that, at the starting times of each cycle, the system is in V, but, during the cycle, the voltage can temporarily escape from V. Such a possible deviance is however limited due to continuity reasons.

Consider a box $V \subset \mathbb{R}^n$ and a time sampling value τ. The controllability method takes a rectangle V as an input, and infers, when it terminates, a subspace $V' = \cup_{i=1}^{m} Control_i$ of V, satisfying: For any $x \in Control_i$, the result of applying mode i to x will lead, after an interval time τ to a point x' which belongs to $Control_j$ for some j. The process can be iterated: the result of applying mode j to x' leads, after a new duration τ, to a point x'' in $Control_k$ for some k, and so on. This shows that, for any starting point $x \in V'$, there is always a sequence of actions $i, j, k, \ldots$ (i.e. a control sequence) that lets the point x inside V at every time $\tau, 2\tau, 3\tau, \ldots$.

The algorithm for generating V' has been described in [6], and is given here in Fig. 9. This Algorithm computes a set of controllable polyhedra. Intuitively, after the k^{th} iteration of the loop, $Control_i$ is a set of states satisfying the following property: there exists a sequence of modes μ of length k starting with mode i such that μ applied to any state of $Control_i$ prevents the system to go out of V at any sampling time; alternatively, after the k^{th} iteration, $Uncontrol$ is a set of states for which, for all sequence μ of length k , there exists a prefix μ' which makes the system go outside V. Note that the termination of the procedure is not guaranteed due to the fact that there are infinitely many polyhedral sets. The proof of correctness of Algoritm 1 is given in [6].

If, given a box $V \subseteq \mathbb{R}^n$, Algorithm 1 outputs the set $\{Control_i\}_{i=1\ldots m}$, one can synthesize an acceptable control for any given initial point $x_0 \in \{Control_i\}$ by simply applying i to x_0 and iterating the process to the resulting point x_1 at next sampling time τ.

Algorithm 1 involves the computation of the Pre-image of convex polyhedra, which is also a convex polyhedra. Unfortunately, Algorithm 1 also involves the computation of union, complementation, and test of equality of polyhedra, that are operations known to be very expensive. To overcome this problem, one can approximate all the manipulated objects using the notion of *griddy polyhedra*, i.e., sets that can be written as unions of closed unit hypercubes with integer vertices, but this leads to an underapproximation the controllability subspace (see [2, 4]).

Input: A box V, a sampling time τ, a switched system Σ with m modes
Output: A controllable subspace $V' = \bigcup_{i=1}^{m} Control_i$

$V' = V$
Repeat
  $Control := V'$
  For $i = 1, \ldots, m$
    $Control_i := \mathrm{Pre}_i(Control) \cap Control$
  End
  $V' := \bigcup_{i=1}^{m} Control_i$
Until $V' = Control$
Return $V' = \bigcup_{i=1}^{m} Control_i$

Fig. 9. Algorithm 1: Synthesis of controllable subspace

Special case of termination after 1 iteration When Algoritm 1 terminates after the first iteration, this means that :
- $\bigcup_{i=1}^{m} Pre_i(V) \supseteq V$.
- $Control_i = V \cap Pre_i(V)$, for all $1 \leq i \leq m$.
- The whole space V is controllable (i.e.: $V' = \bigcup_{i=1}^{m} Control_i = V \cap \bigcup_{i=1}^{m} Pre_i(V) = V$).

In the following, we will see that this special case of termination occurs in the multi-level converters examples.

3 Application to Multi-level Converters

We now consider several examples of n-level converters. These n-level converters are seen as switched systems where the modes correspond to the patterns $Pattern_i$ leading to the generation of one cycle of n-level staircase output signal. We will see on these examples that Algorithm 1 terminates after 1 step. From the constructed sets $Control_{Pattern_i}$, one infers easily a control strategy that maintains the variable $x(t)$ inside V, for each time t of beginning of cycle, whatever the initial value of variable $x(0) \in V$ is.

3.1 Application to 3-level converter

Let us consider the system of Example 1. Let us recall that there are 4 patterns $Pattern_1$, $Pattern_2$, $Pattern_3$ and $Pattern_4$. We chose to keep our system within the following box V: $[98, 102] \times [0, 40]$. (In other words, we want to find a strategy that maintains $98 \leq v \leq 102$ and $0 \leq i \leq 40$.) The application of Algorithm 1 terminates after 1 iteration, and generates the following sets:

- $Control_{Pattern_1}$ is the box delimited by vertices $(98.7, 0); (98.7, 40); (102, 0); (102, 40)$
- $Control_{Pattern_2}$ is the box delimited by vertices $(98, 0); (98, 40); (101.29, 0); (101.29, 40)$

– $Control_{Pattern_3}$ is the box delimited by vertices
$(99.47, 0); (99.47, 40); (102, 0); (102, 40)$
– $Control_{Pattern_4}$ is the box delimited by vertices
$(98, 0); (98, 40); (100.53, 0); (100.53, 40)$

One can see that $Control_{Pattern_3}$ is strictly included into $Control_{Pattern_1}$, and $Control_{Pattern_4}$ into $Control_{Pattern_2}$. Boxes $Control_{Pattern_1}$ and $Control_{Pattern_2}$ are depicted in Fig. 10. As mentioned above, they cover the whole space V which is thus entirely controllable. The control induced by the set $\{Control_i\}_{i=1,\ldots,4}$ consists, at each time t of beginning of cycle, to apply $Pattern_i$ if $x(t)$ belongs to $Control_i$. For example, an acceptable control strategy consists, at each starting time t of a new cycle, to

– apply $Pattern_1$ if $v_1(t) > 98.7$
– apply $Pattern_2$ if $v_1(t) \leq 98.7$.

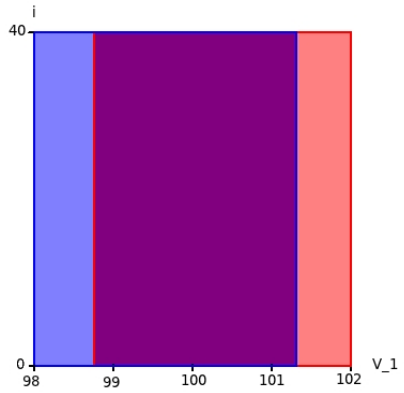

Fig. 10. Controllable area (Red by $Pattern_1$; Blue by $Pattern_2$; Purple by $Pattern_1$ or $Pattern_2$)

Numerical simulation For particular initial values of $x(0)$, one can experimentally check by simulation that the above strategy maintains v_1 between 98V and 102V. For example, for initial point $v_1 = 100$ and $i = 16$, we see, using simulation tool PLECS [1], that:
- the output voltage v_0 has 3-level staircase form (see Fig. 12).
- the capacitor voltage v_1 is maintained between 98V and 102V at each beginning of cycle. See Figures 11 and 13.

As noticed in Sec. 2.2, between two starting times of cycle, the voltage can temporarily escape from the predefined zone V. This can be seen on the left part of Fig. 13 wherethe curb goes slightly below 98V (down to 97.6V).

Fig. 11. Capacitor voltage $v_1(t)$ for the controlled 3-level converter

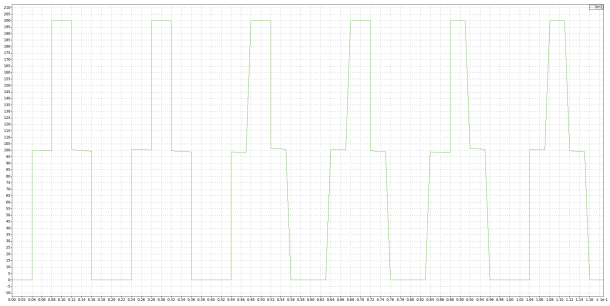

Fig. 12. Output voltage $v_o(t)$ for the controlled 3-level converter

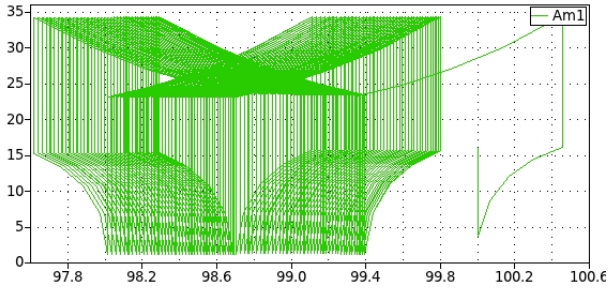

Fig. 13. Trajectory in the phase plane (v_1, i)

3.2 Application to a 4-level Converter

Let us consider the system of Example 2. Let us suppose that V is if the form $\{(v_1, v_2, i) | v_1 \in [196, 204], v_2 \in [96, 104], i \in [0, 60]\}$. For

V, Algorithm 1 terminates after 1 iteration. From the constructed sets $Control_{Pattern_i}$, one easily infers the following strategy:

- Apply pattern $[000, 100, 110, 111, 110, 100, 000]$ if $v_1 \in [196, 200]$ and $v_2 \in [96, 100]$.
- Apply pattern $[000, 010, 110, 111, 011, 010, 000]$ if $v_1 \in [200, 204]$ and $v_2 \in [96, 100]$.
- Apply pattern $[000, 100, 101, 111, 101, 001, 000]$ if $v_1 \in [196, 200]$ and $v_2 \in [100, 104]$.
- Apply pattern $[000, 001, 011, 111, 011, 001, 000]$ if $v_1 \in [200, 204]$ and $v_2 \in [100, 104]$.

Numerical simulation For particular initial values of $x(0)$, one can experimentally check by simulation that the above strategy maintains v_1 (resp. v_2) between 196V and 204V (resp. 96V and 104V). For example, for initial point $v_1 = 196, v_2 = 96$ and $i = 30$, we see, using simulation tool PLECS [1], that:
- the output voltage v_0 has 4-level staircase form (see Fig. 14).
- the capacitor voltage v_1 (resp. v_2) is maintained between 196V and 204V (resp. 96V and 104V) at each beginning of cycle. See Figure 14 and Figure 15.

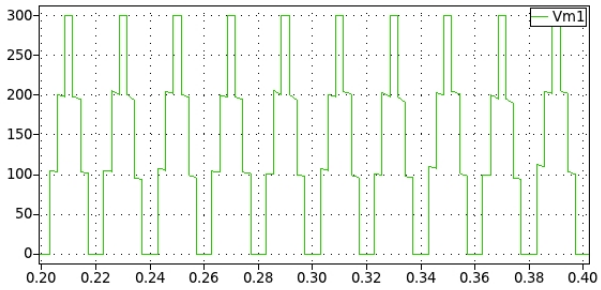

Fig. 14. Output voltage $v_o(t)$ for the controlled 4-level converter

4 Final Remarks

We have shown that the formal methods for synthesizing the controllable subspaces of switched systems can be applied to an important class of power electronics systems: multi-level converters. The method guarantees that the system behaves well for a dense set of initial values for the electric parameters. We plan to apply the method to multi-level converters with a large number of cells, which is today a major challenge for the industry of power electronics.

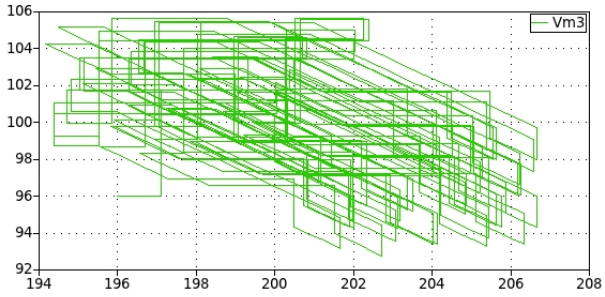

Fig. 15. Trajectory in the phase plane (v_1, v_2) for the 4-level converter

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