COUPLET: Coupled Electrothermal Simulation

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June 2011

Research report LSV-11-18

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Abstract. The aim of the project COUPLET (supported by Institut Farman) is to study the electrothermal effects of the degradation of the metallisation layer of power semiconductor dies. In this first technical report of the project, we describe our work of modeling and simulation of the behavior of a power transistor. The die is represented by four elementary transistors driven by a distributed gate signal. A simplified electrical model is used to simulate the transistor behavior at turn-off. The thermal model is realized by finite elements methods and allows to estimate the maximum temperature on each elementary transistor. By coupling the thermal model with the electric simulation, it is possible to take into account silicon and metallisation heating in the electrical model.

1 Introduction

The study of the electrothermal behavior of semiconductor chips and power modules requires complex model and simulation techniques. Since the temperature is a major factor of ageing of such systems, it is important to improve the accuracy of the models and their simulations.

The problem is difficult because there is an intimate intricacy (coupling) between the electrical and thermal features of the system: First, the electrical components dissipate power, thus rising the temperature; second, the elevation of the temperature induces a modification of the electrical parameters (resistivity, capacity, ...), which, in turn, has an effect on power dissipation.

The coupling between the two phenomena is difficult to simulate since the equations that respectively govern the electrical and the thermal system are different both in terms of nature and numerical resolution: electrical equations are ordinary differential equations (Kirchhoff laws) while thermal equations are partial differential equations (Fourier equations). Accordingly, the methods used for solving these two kind of systems of equations are intrinsically different (typically, finite difference equations on the one hand, finite elements on the other hand). The possible methods of coupling are also multiple, e.g direct method based on modelling of thermal and electronic behavior of the circuit using a single simulation tool, or relaxation methods based on the resolution of the two sets of equations separately using distinct simulators (see e.g. [6]).

The purpose of this paper is to model and simulate the electrothermal behavior in a simple case study of a MOSFET (*metal-oxide-semiconductor field-effect*) transistor. We will study the evolution of the electrical and thermal characteristics of the transistor when it is driven by a periodic square wave voltage.

We will use the tool MATLAB/SIMULINK for simulating the electrical behavior and the tool CASTEM for simulating the thermal behavior. We will simulate the behaviors under normal conditions and under stress (repeated short circuits). We will try to observe the influence and coupling on the thermal subsystem onto the electrical subsystem. We will also try to compare the results of the simulations with the phenomena observed physically (using oscilloscope measures) on the real system implemented in the SATIE laboratory.

The report is structured as follows. First, we will give present some background on the thermal effects on power modules in Section 2. Our case study is introduced in Section 3. In Sections 4 and 5, the electric and thermal model are presented in detail. The results of the coupled simulation is discussed in Section 6, and a short summary is given in Section 7.

2 Background

Figures 1 and 2 show a typical integrated inverter power module in *insulated-gate bipolar transistor* (IGBT) technology, and a schematic view of a typical power modules assembly. As can be seen, such devices are complex multilayered structures with different materials and thus different physical properties.

Each silicon die is constructed by paralleling a large number of elementary transistors (about $10^6/cm^2$).

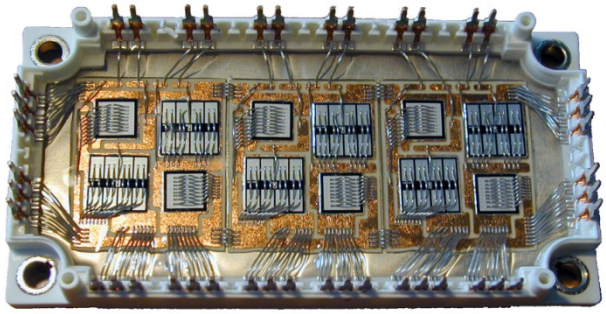


Fig. 1. integrated inverter IGBT power module (200A-600V)

This type of package must provide a good ability for electrical insulation and a good thermal conduction capability for cooling purposes. Such devices are subjected to hard working conditions, especially if they are used in transport systems and automobile applications because of the thermal cycling stress due to

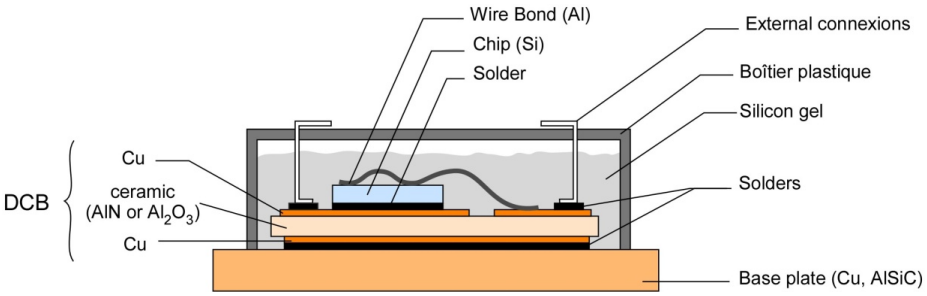


Fig. 2. Schematic view of a typical power module assembly

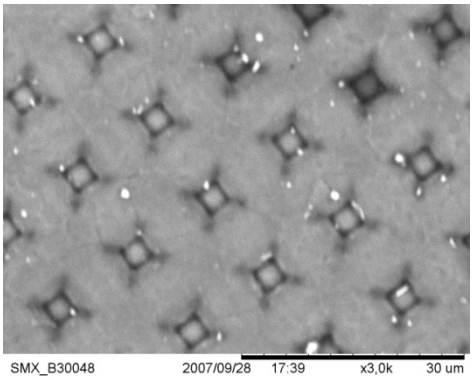


Fig. 3. Elementary cells of a power semiconductor transistor [2]

both environmental conditions and mission profiles. As a consequence, the mismatch of the *coefficient of thermal expansion* (CTE) makes the power module particularly exposed to thermo-mechanical fatigue failures. Table 1 gives material properties of a typical electronic power module. Table 2 gives a summary of failure modes and failure indicators observed during power cycling tests.

To give an impression on occurring electrothermal problems, this section gives some background on the effect of the reconstruction of the emitter metallisation of the chip. This phenomenon is due to large thermal cycling of the die and the CTE mismatch between aluminum material and silicon (Figure 4). When devices are operated cyclically at maximum junction temperature higher than above $110\,°C$, the stress applied in the metal layer exceeds the yield stress and plastic deformation occurs. This leads to grain sliding and modification of the surface structure of the metallisation.

2.1 Metallisation ageing

Hard working conditions may be subjected repetitively to power semiconductor devices, like short-circuit or avalanche operations, depending on the application

Table 1. Typical properties of used material in module packaging

	Material	**CTE** (ppm/K)	(W/mK)
Die	Silicon	2.6	150
	SiC	3.7	390
Ceramic	AlN	3.1	190
	Al_2O_3	5.5	30
Base Plate	Cu	16	390
	AlSiC	6.5 - 12	180 - 220

Table 2. Failure modes and failure indicators observed during power cycling tests for high power IGBT modules

Failure mode	**Failure mechanism**	**Phenomenon location**	**Failure indicator**
Increase of steady-on state voltage	Degradation of external connections	power external connections	V_{cesat}
Increase of steady-on state voltage	Lift-off bond wire	Bond pad or chip metallisation	V_{cesat}
Increase of thermal resistance, increase of T_{jmax}	Solder delamination	Die attach or DBC substrate attach	R_{thjc}, T_{jmax}
Gate leakage appearance	Gate oxide damage	Gate oxide	I_{ges}
Decrease of breakdown voltage	Collector leakage under V_{ces}	Guard ring	I_{ces}
Case/collector insulation default	Ceramic insulation damage	ceramic	Voltage insulation

and the circuit's environment. Thus, the short circuit capability is one of the figures of merit which defines the robustness of the power semiconductor components, especially for IGBT. Insofar as these constraints are sufficiently short (low level of dissipated energy), the devices are able to undergo many of them but not without consequences on their remaining lifespan. Short-circuit requirements make it necessary to know the number of these regimes the components can undergo under given conditions of operation. So, it is important to examine the behavior of power devices under such severe repetitive working conditions. Especially, in order to be able to predict the number of short-circuit pulses that a given device can tolerate before failure, it is necessary to take into account ageing effects and failure indicators on the devices and the associated failure mechanisms.

Figure 5 shows the shorts-circuit robustness of $600\,V$ NPT IGBT transistors where the critical energy (E_C) is $0.81\,J$ at $T_{CASE} = 25\,°C$ and $0.62\,J$ at $T_{CASE} = 125\,°C$. Each point is the result of repetitive tests on a given device, with on the X-axis the dissipated energy and on the Y-axis the number of short-circuit cycles until destruction. This critical value clearly defines two

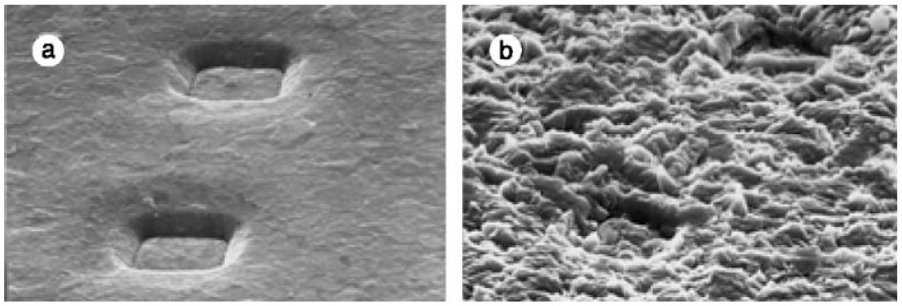


Fig. 4. Aluminum metallisation before power cycling (a) and reconstructed metallisation after power cycling (b) [4]

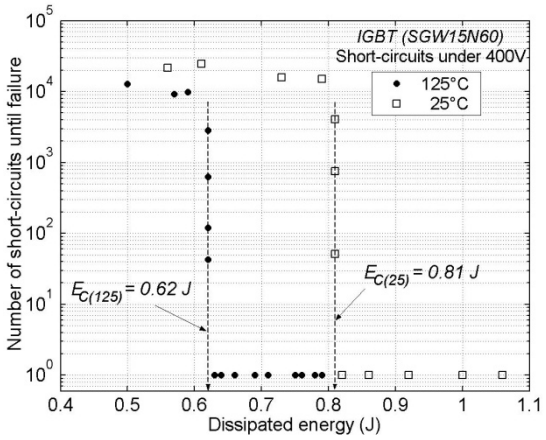


Fig. 5. Robustness in repetitive short-circuit conditions of 600 V NPT IGBT (effect of case temperature) [5]

failure modes depending on whether the short-circuit energy is greater or lower than this singular value.

For dissipated energies greater than the critical value ($E > E_C$), failure occurs during the *first* short circuit and is due to a thermal runaway phenomenon [5].

For short circuit energies below the critical value ($E < E_C$), failure occurs after a large number of short circuits. These results show that a cumulative damaging mechanism occurs in devices ageing which leads to failure after at least 10^4 short circuit cycles. In these conditions, failures systematically appear at turn-off when trying to switch off the short-circuit current (Figure 6) with a destruction phenomenon which looks like dynamic latch-up.

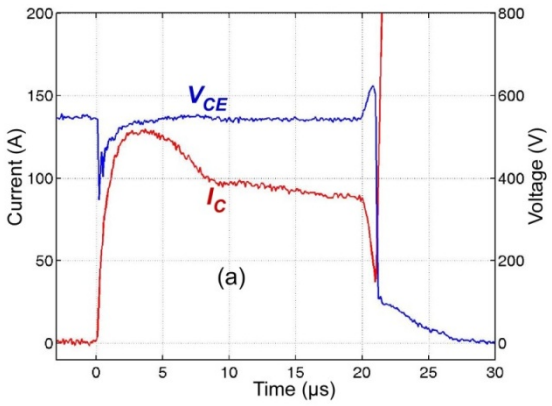


Fig. 6. Waveforms at failure in the case of dissipated energy lower than the critical value (1200 V NPT IGBT, $U = 540$ V, destruction after $N = 33661$ short-circuits) [5]

2.2 Electrical effects of metallisation ageing

The experimental test conditions consist in repetitive short-circuit operations applied to the *device under test* (DUT) with the same energy dissipated in the die until destruction. This energy is supplied by a set of capacitors and a circuit breaker (1200 V 200 A IGBT) that allows to avoid the DUT explosion by an over current detection (200 A). An acquisition card controls the DUT gate drive pulses and allows to stop the tests when a failure is detected. These tests are performed with a gate to emitter voltage of 15 V in the on-state. A repetitive cycle of 0.33 Hz is chosen in order to avoid overheating of the chip. A heating plate allows to control the case temperature and to consider the case temperature influence, especially at 25 °C and 125 °C.

Each 1000 short-circuits, several electrical parameters are measured during the repetition of the short-circuit operations: on-state voltage (V_{CEON}), threshold voltage (V_{GETH}), input/output capacitors (C_{ISS}, C_{OSS}), gate leakage current (I_{GES}), collector leakage current (I_{CESS}) and short-circuit current (I_{SC}). The first three parameters have been measured for 25 °C junction temperature, leakage currents have been measured at 125 °C and short-circuit current during the short-circuit test.

The threshold voltage is measured for different values of emitter current in order to evaluate transconductance evolution (10 μA, 100 μA, 500 μA and 1 mA). The gate leakage current is estimated using a KEITHLEY 6430 SMU. The collector leakage current is measured for a collector to emitter voltage of 200 V (6430 SMU) at 125 °C junction temperature.

Furthermore, in order to set up test campaigns allowing to follow the ageing of tested devices, other electrical parameters must be evaluated. During short-circuit cycles, not only the bulk of the device is strongly thermally constrained but also its immediate vicinity such as aluminum metallisation of emitter pad

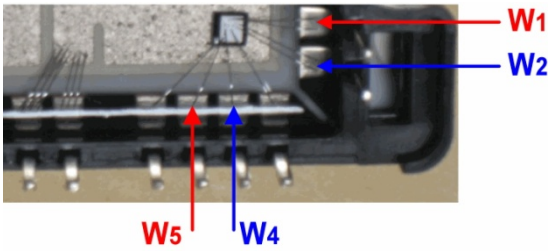


Fig. 7. Dedicated IGBT power module realized by Microsemi

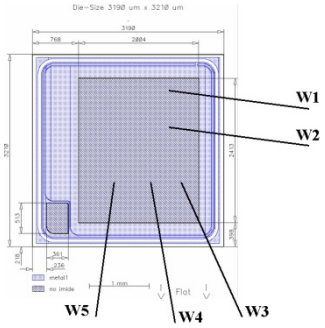


Fig. 8. Bond wire locations on emitter metallisation pad of IGBT die

and bond wires (especially electrical contact between wires and metallisation). In order to characterize the electrical resistances of die metallisation pads as well as contacts between bond wires and metallisation, Microsemi has realized a dedicated package. Several modules with 600 V IGBT dies (in Trench Field Stop technology) have been provided for this study. A four probe contact design was chosen for the bond wire connections (with judicious location of bond contacts) in order to perform precise measurement of the Al metallisation layer (Figures 7 and 8).

Figure 9 gives an example of measurement methodology for Al layer resistance evaluation where $R_{AL_{24}}$ is the Al layer resistance between wires 2 and 4, R_C are the contact resistance between Al layer and bond wire and R_W are the wires resistances.

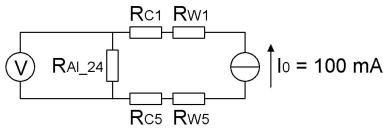


Fig. 9. Example of part of Al layer measurement

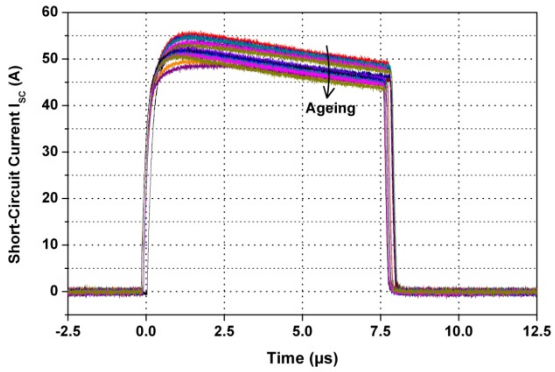


Fig. 10. Decrease of the short circuit current during repetition of SC operations ($T_{CASE} = 125\,^{\circ}C, U = 400\,V$) [5]

Several $600\,V$ IGBT dies were tested in repetitive short-circuit operations and in ageing mode conditions (dissipated energy lower than the critical value). Supply voltage is equal to $400\,V$ and dissipated energy to $156\,mJ$. In the following, results are given for only one device which has failed after 87900 short-circuits. All results obtained with other devices are similar to the presented one. As mentioned above, several electrical parameters have been monitored during ageing tests in order to point out ageing indicators.

On all tested devices, we can note no significant variation of the following characteristics: threshold voltage V_{GETH} for the different chosen emitter current, input/output capacitors (C_{ISS}, C_{OSS}), gate leakage current I_{GES} and collector leakage current I_{CESS}. For example, Figure 6 shows a typical evolution of the threshold voltage measurement.

However, short-circuit waveforms regularly stored during the repetitive short-circuit tests show a significant decrease of the short-circuit current (I_{sc}) before the failure appears, as shown in Figure 10.

On-state voltage is another electrical parameter that presents a regular variation during the tests. Figure 11 shows an increase of the on-state voltage periodically measured during the repetition of the short-circuit operations. Figure 12 presents the evolution of the on-state voltage variation as a function of collector current, $\Delta V_{CEON} = f(I_c)$. The results are presented after 35000 and 70000 short-circuit cycles.

The linear variation of the increasing on-state voltage with the collector current shows an ohmic increase of the voltage. These results show that the ageing effect results in an increase of the on-state voltage which is due to the increase of the on-state resistive part of the voltage. In the same time, and in correlation to the increase of the on-state resistance, short-circuit current regularly decreases during short-circuit repetitions.

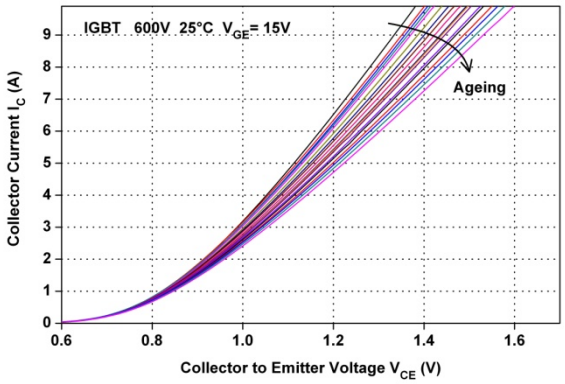


Fig. 11. Increase of the on-state voltage during repetition of SC operations ($T_{CASE} = 25\,°C, V_{GE} = 15\,V$)

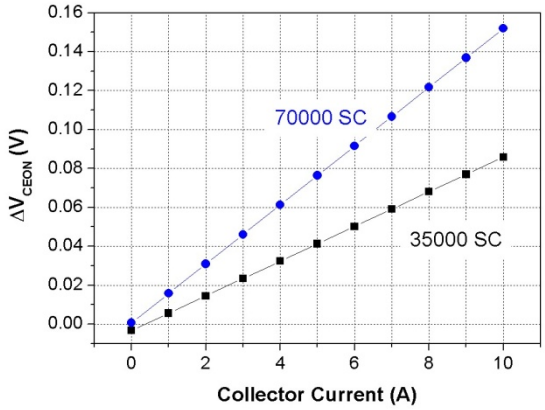


Fig. 12. Voltage variation with current collector after 35000 and 70000 repetitive short-circuit cycles [2]

Elementary cell disconnections resulting from metallisation ageing is one hypothesis which could explain these two results. Another hypothesis is the transconductance variation due to the metallisation degradation as well (increase of the internal source resistance which decreases gate to source voltage). In order to understand ageing phenomena, resistance measurements of the Al layer have been performed as well as failure analyses.

It is well known that Al reconstruction appears in the Al layer when it is subjected to temperature cycles, especially at high temperatures. Due to the large difference between the thermal expansion coefficients for Al and Si, significant plastic deformation occurs in the aluminum layer leading to severe degradations.

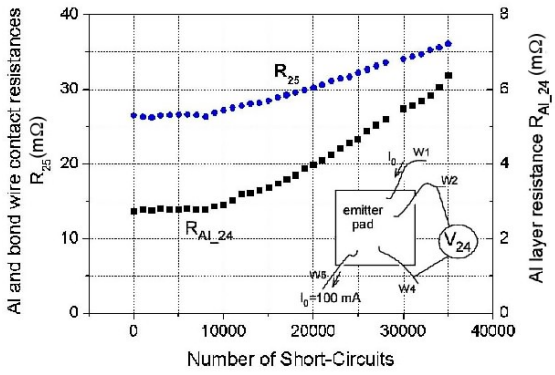


Fig. 13. Evolution of Al layer resistance during repetition of the SC operations (600V NPT IGBT) [2]

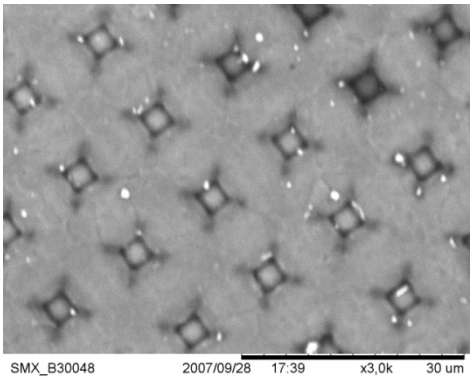
Figure 13 depicts the evolution of the Al metallisation resistance during the repetition of the short circuit operations. Two resistances are drawn in this figure, the Al metallisation resistance between wires 2 and 4 ($R_{Al_{24}}$, see Figure 11) and the resistance R_{25} which is the sum $R_{Al_{25}} + R_{bondcontactwire5} + R_{wire5}$. For these measurements, a small current has been injected between wire 1 and 5 and the voltage have been measured between wires 2 and 4 on one hand and wires 2 and 5 on the other hand.

After about 10,000 short circuits, the resistance of the Al layer significantly and regularly increases until failure occurs (with an increase by a factor of approximately 2.5 for $R_{Al_{24}}$). Contrary to the on-state voltage which consistently increases from the beginning of the tests, about 10,000 cycles are necessary to show a significant evolution of the Al sheet resistance. It seems that these two phenomena are not correlated.

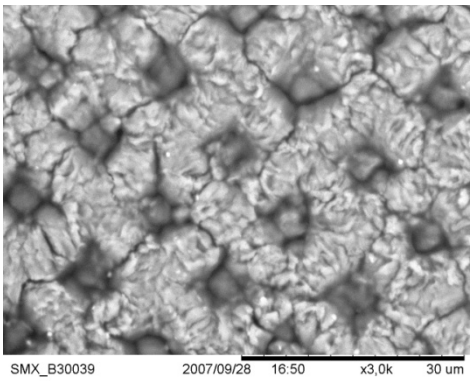
2.3 Failure Analysis

Failure analyses using *scanning electron microscopy* (SEM) have shown that the failure is located to the emitter bond wire contact with significant reconstruction of the Al layer. However, the short-circuit repetition generates thermal cycling in the DUT with high temperature variations. The thermal cycling introduces periodical compressive and tensile stresses in the thin emitter metallisation film due to the CTE mismatch between aluminum ($23.8\,ppm/°C$) and the silicon chip ($2.6\,ppm/°C$). Consequently, stress within the thin aluminum film during repetitive short circuit operations of the device leads to high plastic deformations with dislocation glide.

Figure 14 shows SEM micro graphs of the emitter metallisation before and after tests. A strong degradation of the metallisation after cycling is observed. This degradation causes an increase of the metallisation resistance and weakens the bond wire contacts.



(a) before tests

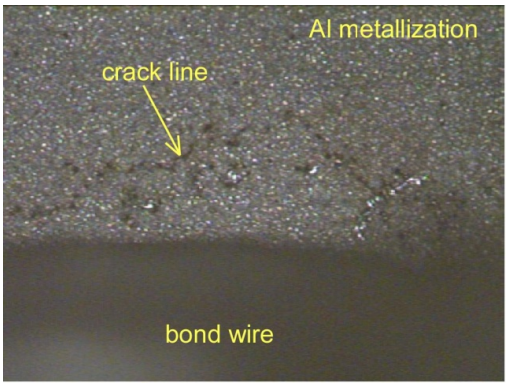


(b) after failure (24600 cycles)

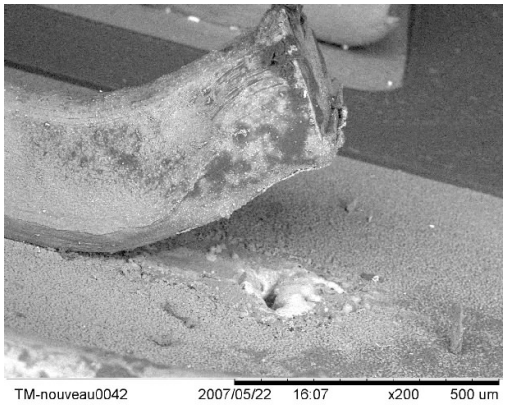
Fig. 14. Al reconstruction after 24600 short-circuit cycles [2]

Cracks also occur around the bond wire contact as shown in Figure 15(a), leading to an increasing contact resistance. In addition, the bond wire contact is probably weakened by thermo-mechanical stress induced by thermal cycling due to the repetitive short-circuits. The degradation of the wire bond contact leads to an increase of the bond contact resistance. As a consequence the local temperature rises, and enforces thermal fatigue. The local temperature increase is large enough to eventually trigger the parasitic transistor of the IGBT and could explain failure at turn-off observed after repeating many short-circuits.

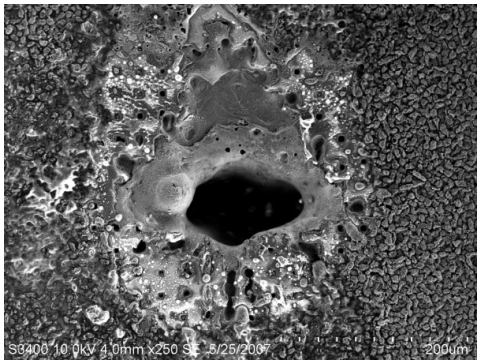
Failure always leads to wire bond lift off (Figure 15(b)) as a consequence of the high current density and of the local melting of the bond end (Figure 15(c)).



(a) Crack around the bond wire contact (optical image, 200x)



(b) Bond wire lift off after failure



(c) Melted hole on the footprint of an aluminum bond wire after lift off

Fig. 15. Various defects [2]

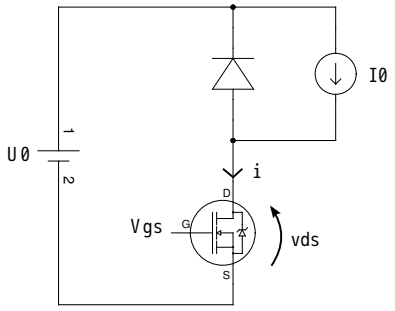


Fig. 16. Overall electric system

3 Examined system

This study is concerned with electrothermal effects of the degradation of the metallisation layer of power semiconductor dies. In a first step, we focus on the behavior of a power transistor at turn-off by modeling the effect of the gate drive propagation on the elementary cells. The die is represented by only 4 elementary transistors driven by a distributed gate signal. A simplified electrical model is used to simulate the transistor behavior at turn-off. The thermal model is realized by finite elements methods and allows to estimate the maximum temperature on each elementary transistor. By coupling the thermal model with the electric simulation, it is possible to take into account silicon and metallisation heating in the electrical model.

3.1 External circuit

The overall electric system is shown in Figure 16. The central device is a transistor. It is controlled by the signal V_{GS}, which is a square wave with an amplitude of $15\,V$ and frequency F. By the current source and the diode, the current through the transistor is limited to I_0. There are basically two operation modes:

(a) if V_{GS} is low, then $v_{ds} = U_0$ and $i = 0$ (*blocking*)
(b) if V_{GS} is high, then $v_{ds} \approx 0$ and $i = I_0$ (*conducting*)

3.2 Overall system behavior

Figure 17 shows a sketch of the system behavior, starting in the state (a) with V_{GS} low at $0\,V$. In this state, the transistor is blocking, thus $v_{ds} = U_0$ and $i = 0$. With the rising edge of V_{GS}, the current starts to increase until it reaches I_0, corresponding to the transition to state (b). Now, all the current is flowing through the semiconductor and the voltage v_{ds} quickly drops to a small value.

At the falling edge of V_{GS}, first the voltage v_{ds} starts to increase until it reaches U_0. Here, the system moves back to state (a) and the current i drops to zero.

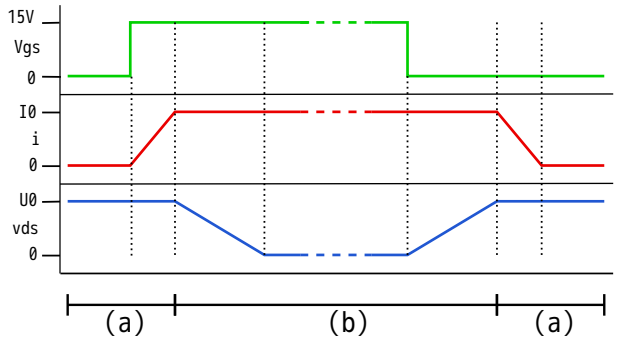


Fig. 17. Sketch of system behavior

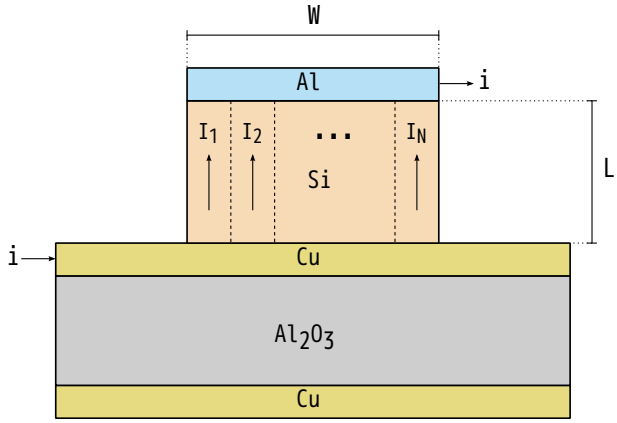


Fig. 18. Transistor geometry

3.3 Transistor geometry

The two-dimensional geometry of the transistor is shown in Figure 18. The current i is flowing from the copper layer through the silicon to the aluminum layer on top. The whole device is placed on an aluminium oxide insulator. The gate is not shown in the figure, it is external to the device, since the current in the silicon is controlled by the electric field induced by V_{GS}. In order to observe the thermal effect on the semiconductor current, the silicon layer is divided into N segments, each of which will have its own current I_n, depending on the local temperature T_n and the voltage v_{gs_n}. To keep the model simple, we consider a global voltage v_{ds}.

Table 3. Parameter values

Name	Value	Name	Value
T_0	$300\ K$	R_G	$1\ \Omega$
V_{T_0}	$5\ V$	R_{Al}	$10 \cdot 10^{-3}\ \Omega$
φ	$8.5 \cdot 10^{-3}\ V/K$	L_G	$100 \cdot 10^{-9}\ H$
μ_0	$200 \cdot 10^{-4}\ m^2V^{-1}s^{-1}$	C_{GS}	$1 \cdot 10^{-9}\ F$
W	$1\ m$	C_{DS}	$100 \cdot 10^{-12}\ F$
L	$2 \cdot 10^{-6}\ m$	C	$100 \cdot 10^{-9}\ F$
C_{ox}	$1.05 \cdot 10^{-3}\ F/m^2$	I_0	$10\ A$
m	-2.42	U_0	$200\ V$
N	4	F	$20\ kHz$

4 Electric model

4.1 Semiconductor

The current in each segment of the semiconductor is defined as follows:

$$I_{Si} = \begin{cases} 0 & , v_{gs} < V_T \\ K\left(2\left(v_{gs} - V_T\right)v_{ds} - v_{ds}^2\right) & , v_{gs} \geq V_T,\ v_{ds} \leq v_{gs} - V_T \\ K\left(v_{gs} - V_T\right)^2 & , v_{gs} \geq V_T,\ v_{ds} \geq v_{gs} - V_T, \end{cases} \tag{1}$$

where K and V_T are functions of the temperature T:

$$V_T = V_{T_0} - \varphi(T - T_0), \tag{2}$$

$$K(T) = \frac{1}{2}\mu(T)\ C_{ox}\frac{W}{L \cdot N}, \tag{3}$$

$$\mu(T) = \mu_0 \left(\frac{T}{T_0}\right)^{-m}. \tag{4}$$

Each current I_n depends on the global voltage v_{ds}, the local voltage v_{gs_n} and the local temperature T_n. The current I is the sum of these currents:

$$I_n = I_{Si}(v_{ds}, v_{gs_n}, T_n), \quad I = \sum_{n=1}^{N} I_n.$$

During normal operation of the system, the current through the transistor is limited to I_0. Using the parameters shown in Table 3, the characteristics of the transistor is shown in Figure 19.

4.2 Circuit model

The model of the internals of the transistor is shown in Figure 20. The gate voltage V_{GS} is distributed over the N partitions as voltages v_{gs_n}. At the input V_{GS}, there is a small inductance L with its corresponding current i_L. There is

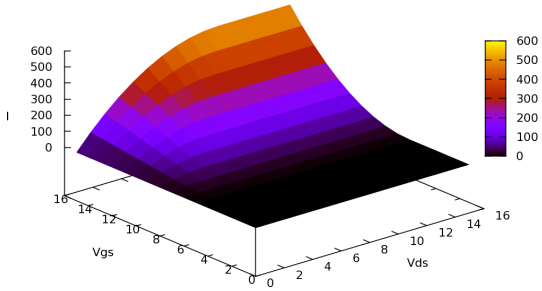


Fig. 19. Transistor characteristics

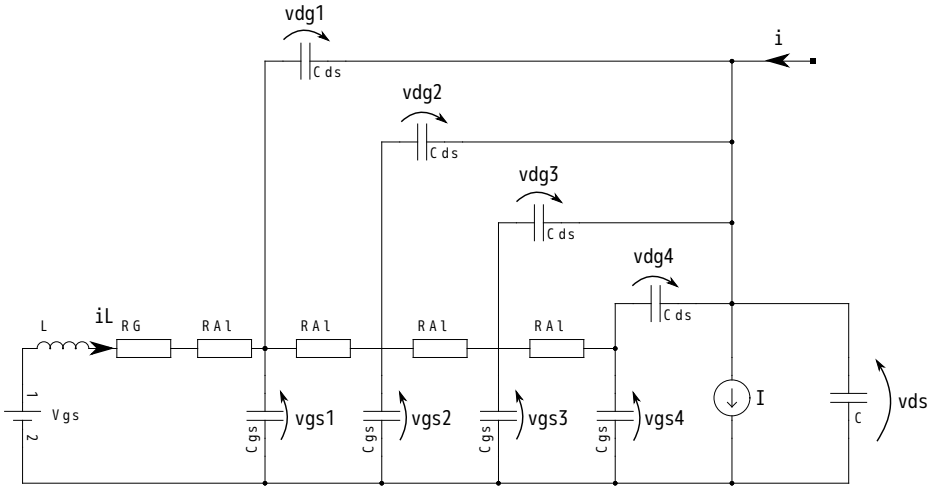


Fig. 20. Circuit structure

a gate resistance R_G, and resistances R_{Al} in each of the N segments. In each segment, gate and source are coupled with a capacitance C_{GS}, while gate and drain are coupled with C_{DS}. The current source I is in fact the sum of the N currents in the semiconductor (cf. Figure 18), which are determined by the nonlinear semiconductor equations described in the previous section.

As state variables in the circuit model, we have the voltage v_{ds}, the inductor current i_L and the voltages v_{gs_n} and v_{dg_n}. The input voltage is V_{GS}, and there are the currents I_0 (not in the schema of Figure 20) and I, acting as inputs. As output variables, we have the voltages $v_{ds}, v_{gs_1} \dots v_{gs_N}$ and the current i. This gives us the input, state and output vectors u, x and y, respectively:

$$
\begin{aligned}
u =& [V_{GS}, I_0, I]^T, \\
x =& [v_{ds}, i_L, v_{gs_1} \dots v_{gs_N}, v_{dg_1} \dots v_{dg_N}]^T, \\
y =& [v_{ds}, v_{gs_1} \dots v_{gs_N}, i]^T.
\end{aligned}
$$

According to the two different states of the overall system, we have two systems of differential equations that determine the behavior of the circuit. In phase (a), v_{ds} is fixed at U_0, while i is floating depending on the currents i_{dg_n}, i_{ds} and I. In phase (b), i is fixed at I_0 and v_{ds} depends on v_{dg_n} and v_{gs_n}. In the following, we give the differential equations for $N = 4$ segments.

The first equations implement the behavior of the two phases described in the previous paragraph:

$$\frac{dv_3}{dt} = 0, \tag{5a}$$

$$I_0 = I \ + C\frac{dv_{ds}}{dt} \ + \ \sum_{n=1}^{4} C_{DS}\frac{dv_{dg_n}}{dt}. \tag{5b}$$

The remaining equations describing the system state are independent of the phase of the system. According to the voltage law applied on the loop along V_{GS}, the inductance and the first capacitance v_{gs_1}, we have

$$V_{GS} = L_G\frac{di_L}{dt} + (R_G + R_{Al})i_L + v_{gs_1}. \tag{6}$$

For the four nodes joining v_{gs_n} and v_{dg_n}, we have

$$C_{GS}\frac{dv_{gs_1}}{dt} + \frac{v_{gs_1} - v_{gs_2}}{R_{Al}} = i_L + C_{DS}\frac{dv_{dg_1}}{dt} \tag{7}$$

$$C_{GS}\frac{dv_{gs_2}}{dt} + \frac{v_{gs_2} - v_{gs_3}}{R_{Al}} = \frac{v_{gs_1} - v_{gs_2}}{R_{Al}} + C_{DS}\frac{dv_{dg_2}}{dt} \tag{8}$$

$$C_{GS}\frac{dv_{gs_3}}{dt} + \frac{v_{gs_3} - v_{gs_4}}{R_{Al}} = \frac{v_{gs_2} - v_{gs_3}}{R_{Al}} + C_{DS}\frac{dv_{dg_3}}{dt} \tag{9}$$

$$C_{GS}\frac{dv_{gs_4}}{dt} = \frac{v_{gs_4} - v_{gs_3}}{R_{Al}} + C_{DS}\frac{dv_{dg_4}}{dt} \tag{10}$$

Finally, v_{ds} can be rewritten as the sum of each pair $v_{gs_n} + v_{dg_n}$. This implies in form of the derivatives

$$\frac{dv_{ds}}{dt} = \frac{dv_{gs_1}}{dt} + \frac{dv_{dg_1}}{dt}, \tag{11}$$

$$\frac{dv_{ds}}{dt} = \frac{dv_{gs_2}}{dt} + \frac{dv_{dg_2}}{dt}, \tag{12}$$

$$\frac{dv_{ds}}{dt} = \frac{dv_{gs_3}}{dt} + \frac{dv_{dg_3}}{dt}, \tag{13}$$

$$\frac{dv_{ds}}{dt} = \frac{dv_{gs_4}}{dt} + \frac{dv_{dg_4}}{dt}. \tag{14}$$

For the output i, there are two equations depending on the overall system state:

$$i = I \ + C\frac{dv_{ds}}{dt} \ + \ \sum_{n=1}^{4} C_{DS}\frac{dv_{dg_n}}{dt}, \tag{15a}$$

$$i = I_0. \tag{15b}$$

To obtain convenient state equations in the form $\dot{x} = Ax + Bu$, we rewrite the above equations as follows:

$$Q_a \cdot \dot{x} = \tilde{A} \cdot x + \tilde{B}_a \cdot u,$$
$$Q_b \cdot \dot{x} = \tilde{A} \cdot x + \tilde{B}_b \cdot u, \text{ where}$$

$$\tilde{A} = \begin{pmatrix} 0 & \dots & \dots & \dots & \dots & \dots & \dots & 0 \\ 0 & -(R_G + R_{Al}) & -1 & 0 & \dots & \dots & \dots & 0 \\ 0 & 1 & -\frac{1}{R_{Al}} & \frac{1}{R_{Al}} & 0 & \dots & \dots & 0 \\ 0 & 0 & \frac{1}{R_{Al}} & -\frac{2}{R_{Al}} & \frac{1}{R_{Al}} & 0 & \dots & 0 \\ 0 & 0 & 0 & \frac{1}{R_{Al}} & -\frac{2}{R_{Al}} & \frac{1}{R_{Al}} & 0 \dots & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{R_{Al}} & -\frac{2}{R_{Al}} & 0 \dots & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \dots & 0 \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \dots & 0 \end{pmatrix},$$

$$\tilde{B}_a = \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \\ \vdots & & \vdots \\ 0 & 0 & 0 \end{pmatrix}, \quad \tilde{B}_b = \begin{pmatrix} 0 & 1 & -1 \\ 1 & 0 & 0 \\ 0 & 0 & 0 \\ \vdots & & \vdots \\ 0 & 0 & 0 \end{pmatrix},$$

$$Q_a = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & L_G & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & C_{GS} & 0 & 0 & 0 & -C_{DS} & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{GS} & 0 & 0 & 0 & -C_{DS} & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{GS} & 0 & 0 & 0 & -C_{DS} & 0 \\ 0 & 0 & 0 & 0 & 0 & C_{GS} & 0 & 0 & 0 & -C_{DS} \\ 1 & 0 & -1 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ 1 & 0 & 0 & -1 & 0 & 0 & 0 & -1 & 0 & 0 \\ 1 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & -1 & 0 \\ 1 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & -1 \end{pmatrix},$$

$$Q_b = \begin{pmatrix} C & 0 & 0 & 0 & 0 & 0 & C_{DS} & C_{DS} & C_{DS} & C_{DS} \\ 0 & L_G & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & C_{GS} & 0 & 0 & 0 & -C_{DS} & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{GS} & 0 & 0 & 0 & -C_{DS} & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{GS} & 0 & 0 & 0 & -C_{DS} & 0 \\ 0 & 0 & 0 & 0 & 0 & C_{GS} & 0 & 0 & 0 & -C_{DS} \\ 1 & 0 & -1 & 0 & 0 & 0 & -1 & 0 & 0 & 0 \\ 1 & 0 & 0 & -1 & 0 & 0 & 0 & -1 & 0 & 0 \\ 1 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & -1 & 0 \\ 1 & 0 & 0 & 0 & 0 & -1 & 0 & 0 & 0 & -1 \end{pmatrix}$$

Multiplying from the left with the inverse of Q_a (respectively Q_b) gives

$$\dot{x} \;=\; \left[Q_a^{-1}\tilde{A}\right]\cdot x + \left[Q_a^{-1}\tilde{B_a}\right]\cdot u \;=\; A_a\cdot x + B_a\cdot u \tag{16a}$$

$$\dot{x} \;=\; \left[Q_b^{-1}\tilde{A}\right]\cdot x + \left[Q_b^{-1}\tilde{B_b}\right]\cdot u \;=\; A_b\cdot x + B_b\cdot u \tag{16b}$$

For the output y, we have

$$y = C_a\cdot x + D_a\cdot u, \tag{17a}$$

$$y = C_b\cdot x + D_b\cdot u, \text{ where} \tag{17b}$$

$$C_a = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ z_1 & z_2 & z_3 & z_4 & z_5 & z_6 & z_7 & z_8 & z_9 & z_{10} \end{pmatrix},$$

$$C_b = \begin{pmatrix} 1\,0\,0\,0\,0\,0\,0\,0\,0\,0 \\ 0\,0\,1\,0\,0\,0\,0\,0\,0\,0 \\ 0\,0\,0\,1\,0\,0\,0\,0\,0\,0 \\ 0\,0\,0\,0\,1\,0\,0\,0\,0\,0 \\ 0\,0\,0\,0\,0\,1\,0\,0\,0\,0 \\ 0\,0\,0\,0\,0\,0\,0\,0\,0\,0 \end{pmatrix},$$

$$D_a = \begin{pmatrix} 0 & 0 & 0 \\ \vdots & & \vdots \\ 0 & 0 & 0 \\ w_1 & w_2 & w_3+1 \end{pmatrix}, \quad D_b = \begin{pmatrix} 0\,0\,0 \\ \vdots\;\; \vdots \\ 0\,0\,0 \\ 0\,1\,0 \end{pmatrix}.$$

Here, the last rows of C_a and D_a correspond to Equation (15a). Equation (16a) can be used to substitute the derivatives:

$$\begin{aligned} i \;&= I \;+ C\frac{dv_{ds}}{dt} \;+\; \sum_{n=1}^{4} C_{DS}\frac{dv_{dg_n}}{dt} \\ &= I \;+ C\left(\sum_{j=1}^{10}\left[A_a\right]_{1,j} x_j + \sum_{j=1}^{3}\left[B_a\right]_{1,j} u_j\right) \\ &\quad + C_{DS}\sum_{n=1}^{4}\left(\sum_{j=1}^{10}\left[A_a\right]_{6+n,j} x_j + \sum_{j=1}^{3}\left[B_a\right]_{6+n,j} u_j\right) \end{aligned}$$

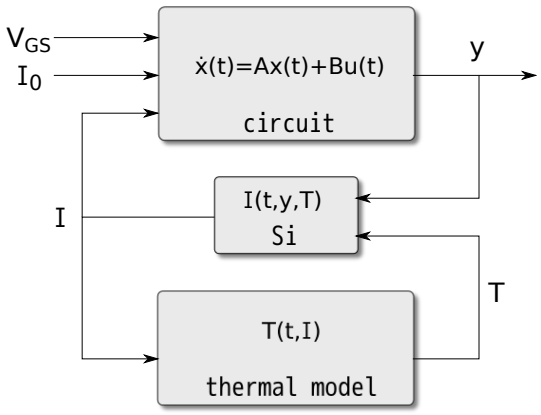


Fig. 21. System model

Thus, we have

$$z_j = C \cdot [A_a]_{1,j} + C_{DS} \sum_{n=7}^{10} [A_a]_{n,j}\,,$$
$$w_j = C \cdot [B_a]_{1,j} + C_{DS} \sum_{n=7}^{10} [B_a]_{n,j}\,.$$

4.3 Electric system model

The state equations (16) and output equations (17) describe two time-invariant linear systems. The switching between the two different phases depends on the system state (see Section 3.2), which makes our system a hybrid or switched system. This will be described by a switching function $\sigma(t)$, which determines the choice of the respective matrices. In the following, we use the notation A_σ, meaning

$$A_\sigma = \begin{cases} A_a & \text{if } \sigma = 0, \\ A_b & \text{if } \sigma = 1. \end{cases}$$

Furthermore, there is a non-linear feedback hidden in the input vector u, more precisely in the semiconductor current I. This current is the sum of the currents $I_1 \ldots I_N$, where each I_n depends in turn on v_{ds}, v_{gs_n} and the temperature T_n (cf. Equation (1)).

In order to make this dependency more explicit, the state and output equations are rewritten as

$$\dot{x}(t) = A_\sigma \cdot x(t) + B_\sigma \cdot \mathcal{U}(t, y, T), \tag{18}$$
$$y(t) = C_\sigma \cdot x(t) + D_\sigma \cdot \mathcal{U}(t, y, T). \tag{19}$$

Here, $\mathcal{U}(t)$ is a function of the output[4] $y(t)$ and the temperature vector $T = [T_1, \ldots, T_N]^T$, given as

$$\mathcal{U}(t, y, T) = \left[V_{GS},\ I_0,\ \sum_{n=1}^{N} I_{Si}(v_{ds}(t), v_{gs_n}(t), T_n(t)) \right]^T . \tag{20}$$

This gives the overall structure of the formalized model as depicted in Figure 21. The details of the thermal model will be described in the following section.

5 Thermal model

5.1 Geometry

In the idealized geometry given in figure 22, one can distinguish different materials. From the thermal point of view, the component is a domain Ω, which can be decomposed into four subdomains corresponding to the four materials used (copper, aluminium oxide, silicon, aluminum).

$$\Omega = \Omega_{Cu} \cup \Omega_{Al_2O_3} \cup \Omega_{Si} \cup \Omega_{Al} \tag{21}$$

Some subdomains are divided in turn into several sub-subdomains. The copper is divided into two zones $\Omega_{Cu,1}$ and $\Omega_{Cu,2}$, corresponding to the two parts surrounding the aluminium oxide layer:

$$\Omega_{Cu} = \Omega_{Cu,1} \cup \Omega_{Cu,2} \tag{22}$$

The silicon is divided into $N + 1$ zones corresponding to different thermal loadings due to the different currents i_n.

$$\Omega_{Si} = \cup_{n=0}^{N} \Omega_{Si,n} \tag{23}$$

In the same way, the aluminum layer is divided into N zones corresponding to different thermal loadings due to the different currents i_n.

$$\Omega_{Al} = \cup_{n=1}^{N} \Omega_{Al,n} \tag{24}$$

The boundary of Ω is denoted $\partial\Omega$. $\partial\Omega = \partial_N\Omega \cup \partial_D\Omega$ is divided in two zones for the definition of the classical Neuman and Dirichlet boundary conditions.

5.2 Heat equations

The thermal problem is a classical dynamic heat problem submitted to imposed temperature, fluxes, and sources linked to the current inside the component. Let us call $T(\mathbf{x}, t)$ the field of temperature defined on $\Omega \times [t_0, t_f]$, where $\mathbf{x}$ denotes

[4] Note that for the relevant variables v_{ds} and v_{gs_n}, the ouput $y(t)$ is identical to the state $x(t)$.

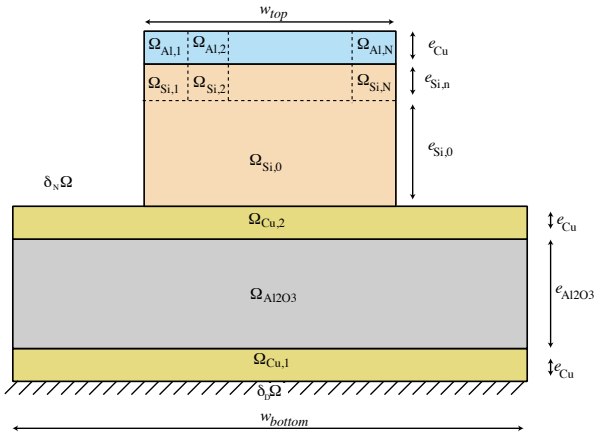


Fig. 22. Domain decomposition for Ω

the position and t the time. The initial (resp. final) time of the study is denoted by t_0 (resp. t_f).

The following governing equations are defined in each subdomain:

$$\forall \mathbf{x} \in \Omega_{Cu}, \forall t \in [t_0, t_f]$$
$$\rho_{Cu} c_{Cu} \frac{\partial T(\mathbf{x},t)}{\partial t} - div(k_{Cu}\mathbf{grad}(T(\mathbf{x},t))) = 0, \tag{25}$$

where ρ_{Cu}, c_{Cu} and k_{Cu} are respectively the volumetric mass, thermal capacity and the thermal conductivity of copper.

$$\forall \mathbf{x} \in \Omega_{Al_2O_3}, \forall t \in [t_0, t_f] :$$
$$\rho_{Al_2O_3} c_{Al_2O_3} \frac{\partial T(\mathbf{x},t)}{\partial t} - div(k_{Al_2O_3}\mathbf{grad}(T(\mathbf{x},t))) = 0, \tag{26}$$

where $\rho_{Al_2O_3}$, $c_{Al_2O_3}$ and $k_{Al_2O_3}$ are respectively the volumetric mass, thermal capacity and the thermal conductivity of aluminium oxide.

$$\forall \mathbf{x} \in \Omega_{Si,0}, \forall t \in [t_0, t_f] :$$
$$\rho_{Si} c_{Si} \frac{\partial T(\mathbf{x},t)}{\partial t} - div(k_{Si}\mathbf{grad}(T(\mathbf{x},t))) = 0, \tag{27}$$

where ρ_{Si}, c_{Si} and k_{Si} are respectively the volumetric mass, thermal capacity and the thermal conductivity of silicon.

$$\forall \mathbf{x} \in \Omega_{Si,j\in\{1,2,\dots N\}}, \forall t \in [t_0, t_f] :$$
$$\rho_{Si} c_{Si} \frac{\partial T(\mathbf{x},t)}{\partial t} - div(k_{Si}\mathbf{grad}(T(\mathbf{x},t))) = g_{Si,j}(t), \tag{28}$$

where

$$g_{Si,j}(t) = \frac{N}{w_{top} e_{Si,n}} v_{ds}.i_{ds_j} \tag{29}$$

$g_{Si,j}(t)$ is a heat source due to the Joule effect and i_{ds_j} is the current relative to tension v_{ds_j}.

$$\forall \mathbf{x} \in \Omega_{Al,j\in\{1,2,...N\}}, \forall t \in [t_0, t_f] :$$
$$\rho_{Al} c_{Al} \frac{\partial T(\mathbf{x},t)}{\partial t} - div(k_{Si} \mathbf{grad}(T(\mathbf{x},t))) = g_{Al,j}(t), \tag{30}$$

where ρ_{Al}, c_{Al} and k_{Al} are respectively the volumetric mass, thermal capacity and the thermal conductivity of aluminium. Finally,

$$g_{Al,j}(t) = \frac{r_{Al}}{e_{Al}^2} \sum_{n=1}^{n=j} i_{ds_n}^2(t), \tag{31}$$

where $g_{Al,j}(t)$ is a heat source due to the Joule effect.

Equations (25, 26, 27, 28, 30) can be gathered into one equation :

$$\forall \mathbf{x} \in \Omega, \forall t \in [t_0, t_f] :$$
$$\rho(\mathbf{x}) c(\mathbf{x}) \frac{\partial T(\mathbf{x},t)}{\partial t} - div(k(\mathbf{x}) \mathbf{grad}(T(\mathbf{x},t))) = g(\mathbf{x},t) \tag{32}$$

where $\rho(\mathbf{x})$, $c(\mathbf{x})$ and $k(\mathbf{x})$ and g($\mathbf{x}$,t) are piecewise constant over each subdomain.

5.3 Boundary and initial conditions

The structure Ω is submitted to imposed temperature on $\partial_D \Omega$:

$$\forall \mathbf{x} \in \partial_D \Omega, \forall t \in [t_0, t_f] :$$
$$T(\mathbf{x},t) = T_0 \tag{33}$$

Fluxes on $\partial_N \Omega$ are null :

$$\forall \mathbf{x} \in \partial_N \Omega, \forall t \in [t_0, t_f] :$$
$$\mathbf{grad}(T(\mathbf{x},t)).\mathbf{n} = 0 \tag{34}$$

Initial temperature on Ω is assumed uniform:

$$\forall \mathbf{x} \in \partial_N \Omega :$$
$$T(\mathbf{x},t_0) = T_0 \tag{35}$$

Table 4. Parameter values for thermal problem

Name	Value
e_{Cu}	200 μm
$e_{Al_2O_3}$	380 μm
$e_{Si,0}$	150 μm
$e_{Si,n}$	50 μm
e_{Al}	3 μm
w_{bottom}	5 cm
w_{top}	1 cm

Name	Value
ρ_{Cu}	8700 kg/m^3
$\rho_{Al_2O_3}$	3970 kg/m^3
ρ_{Si}	2330 kg/m^3
ρ_{Al}	2700 kg/m^3
c_{Cu}	385 $J \cdot kg^{-1} \cdot K^{-1}$
$c_{Al_2O_3}$	780 $J \cdot kg^{-1} \cdot K^{-1}$
c_{Si}	700 $J \cdot kg^{-1} \cdot K^{-1}$
c_{Al}	900 $J \cdot kg^{-1} \cdot K^{-1}$

Name	Value
k_{Cu}	400 $W \cdot m^{-1} \cdot K^{-1}$
$k_{Al_2O_3}$	30 $W \cdot m^{-1} \cdot K^{-1}$
k_{Si}	148 $W \cdot m^{-1} \cdot K^{-1}$
k_{Al}	160 $W \cdot m^{-1} \cdot K^{-1}$
T_0	298 K
r_{Al}	100 $\Omega \cdot m^2$

5.4 Weak formulation

The weak formulation of Equations (32)–(35) can then be written:

$$\begin{aligned} &\text{Find} T(\mathbf{x}) \in \mathcal{T} + \{T_0\}\,, \text{ such that:} \\ &\qquad \forall t \in [t_0, t_f], \\ &\int_\Omega \rho(\mathbf{x}) c(\mathbf{x}) \frac{\partial T(\mathbf{x},t)}{\partial t} v dV + \int_\Omega k(\mathbf{x}) \mathbf{grad}(T(\mathbf{x},t)).\mathbf{grad}(v) dV \\ &\qquad = \int_\Omega g(\mathbf{x},t) v dV \quad , \quad \forall v \in \mathcal{T} \\ &\qquad \text{and } T(\mathbf{x},t_0) = T_0 \text{ on } \Omega, \end{aligned} \tag{36}$$

where $\mathcal{T} = \{v \in \mathcal{H}^1(\Omega) \text{ such that } v = 0 \text{ on } \partial_D \Omega\}$.

5.5 Simulation

The numerical values used in the simulation are given in Table 4. For the numerical simulation of equation (36) we use a standard finite element method for the space discretization (Figure 23) and a classical θ-scheme for the time discretization [3].

Space discretization. We introduce a discretization in space:

$$T(\mathbf{x},t) = \sum_i^{N_{space}} T_i(t) \varphi_i(\mathbf{x}) \tag{37}$$

where N_{space} is the number of finite element shape functions used to discretize and $\varphi_i(\mathbf{x})$ the finite element shapes functions.
We then define a subspace $\mathcal{T}_h \subset \mathcal{T}$:

$$\mathcal{T}_h = \{v \in \mathcal{T} \cap Span(\varphi_{i \in \{1, N_{space}\}})\} \tag{38}$$

Equation (36) can be written as follows:

$$\begin{aligned} &\text{Find} T(\mathbf{x}) \in \mathcal{T}_h + \{T_0\}\,, \text{ such that:} \\ &\forall t \in [t_0, t_f], \\ \int_\Omega \rho(\mathbf{x}) c(\mathbf{x}) \frac{\partial T(\mathbf{x},t)}{\partial t} v dV + \int_\Omega k(\mathbf{x}) \mathbf{grad}(T(\mathbf{x},t)).\mathbf{grad}(v) dV \\ = \int_\Omega g(\mathbf{x},t) v dV \quad , \quad \forall v \in \mathcal{T}_h \\ \text{and } T(\mathbf{x},t_0) = T_0 \text{ on } \Omega \end{aligned} \tag{39}$$

Equation (39) can be written:

$$\begin{aligned} &\text{Find } \underline{T}(t) \in \mathbb{R}^{N_{space}}, \text{ such that:} \\ &\forall t \in [t_0, t_f]: \\ &\mathbb{M}\dot{\underline{T}}(t) + \mathbb{C}\underline{T}(t) = \underline{F}(t), \end{aligned} \tag{40}$$

where $\underline{T}(t)$ is the column vector gathering the nodal values $T_i(t)$ for $i \in \{1, N_{space}\}$ of the temperature.

The mass matrix $\mathbb{M}$ is written:

$$M_{ij} = \int_\Omega \rho(\mathbf{x}) c(\mathbf{x}) \varphi_i(\mathbf{x}) \varphi_j(\mathbf{x}) dV \tag{41}$$

The conductivity matrix $\mathbb{C}$ written :

$$C_{ij} = \int_\Omega k(\mathbf{x}).\mathbf{grad}(\varphi_i(\mathbf{x})).\mathbf{grad}(\varphi_j(\mathbf{x}))\, dV \tag{42}$$

Time discretization. N_{time} discrete instants are introduced on $[0, t_f]$, such that :

$$\begin{aligned} \Delta &= \frac{t_f - t_0}{N_{time}} \\ t_n = t_0 + n\Delta t, &\text{ with } n \in \{1, ..., N_{space}\} \\ \underline{T}_n &= \underline{T}(t_n) \end{aligned} \tag{43}$$

where Δt is the time step.

A classical θ-scheme is then used to compute $\underline{T}_n$, equation (40) then becomes:

$$\mathbb{M}\frac{1}{\Delta t}\left(\underline{T}_{n+1} - \underline{T}_n\right) + \mathbb{C}\left(\theta\underline{T}_{n+1} + (1-\theta)\underline{T}_n\right) = \left(\theta\underline{F}_{n+1} + (1-\theta)\underline{F}_n\right) \tag{44}$$

One obtains an explicit method choosing $\theta = 0$ or an implicit method choosing $\theta = 1$. Choosing $\theta \geq 0.5$ offers unconditional stability of the algorithm.

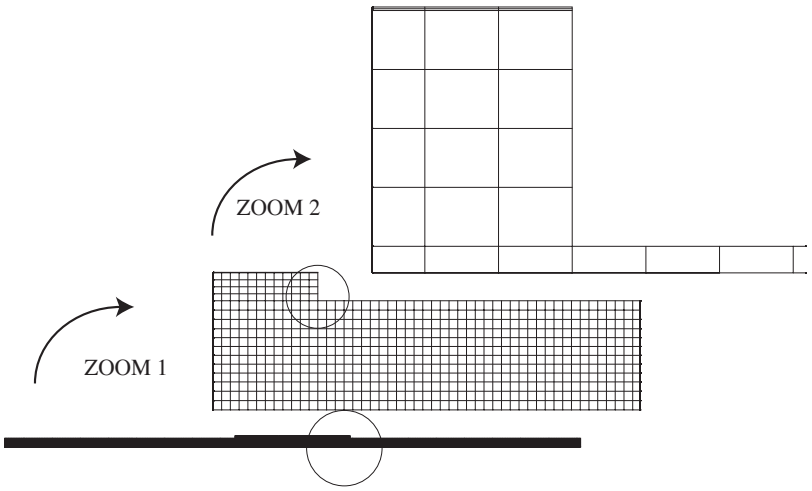


Fig. 23. Mesh used to discretize Ω

6 Coupled Simulation

6.1 Coupled simulation scheme

The above system has been implemented in *Matlab/Simulink*, while the thermal model of the transistor is implemented using the finite elements tool *Castem* [1]. The resolution of the electric model follows an explicit scheme, while the thermal model is in implicit form. The coupled simulation will therefore be performed in an interleaved fashion. Figure 24 shows the simulation scheme. In the figure, E represents the electric simulation, while T relates to the thermal simulation. The two processes communicate via a *first-in-first-out* channel (*FIFO*).

In the initial state (at t_0), all temperatures are assumed to be equal to T_0. The electric simulation performs one time step of length τ, while the thermal simulator is idle. Then (at t_1), the current values of I and v_{ds} are sent via the FIFO to the thermal simulator. With these values, the thermal simulation performs a step of τ as well, reaching t_1, while the electric simulation remains in a waiting state. Having finished its computation, the thermal simulator sends the new temperatures T to the electric model, completing the first step.

Note that in explicit form, a very small τ may be needed to guarantee convergence of the electric simulation ($\tau \approx 10^{-11}\,s$ for the parameters in Table 3). On the other hand, the thermal effects take place on a much larger time-scale ($10^{-3}\,s$ to $1\,s$). Exchanging data after each τ would be very expensive. Thus,

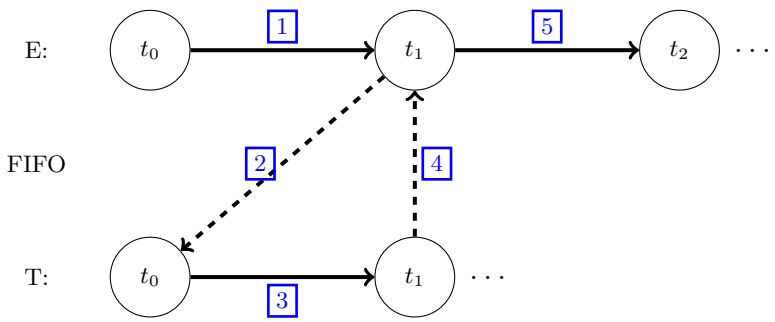


Fig. 24. Interleaved simulation scheme

the sample time for synchronizing the simulators will not be identical to the internal time step for resolving the electric model. Instead, a variable time step solver is chosen within *Simulink* to guarantee convergence at low cost, while the simulation processes are synchronized at a static sample time τ_s. Since under normal conditions, the temperatures change very slowly compared to the electric values, we expect that the error introduced by this approximation is negligible if τ_s is chosen small enough.

6.2 Results

First the phase changes of V_{GS} are simulated on a short time scale, while the temperature is kept constant at T_0. The simulation runs for the rising and falling edge are shown in Figure 25. The respective edge is located at $t = 0.1\,\mu s$.

On a slightly larger timescale, the coupled simulation is run. The simulators are synchronized every $\tau_s = 5\,\mu s$ and the total simulation time is one millisecond. Using a frequency of $20\,kHz$ for the control input V_{GS}, this corresponds to 20 periods. Figure 26(a) shown the values of the four semiconductor currents[5] and the respective temperatures in the four segments.

The curve achieving the highest temperature corresponds to segment $n = 4$, while the coldest segment is the first one. Looking back at the geometry of the transistor in Figure 18, this can be explained as follows. The semiconductor currents I_n flow from the copper layer in vertical direction into the aluminum layer, where they flow to the output on the right hand side. Thus, the current in the aluminum layer above segment n equals the sum of the semiconductor currents $\sum_{j=1}^{n} I_j$. The strongest current will be observed in segment N, which will heat up the fastest.

As expected, in the normal operation of the circuit, the temperatures react very slowly compared to the electrical values. After the total simulation time of $1\,ms$, the temperature in the fourth segment only increased by $0.04\,K$. Nevertheless, a spread in the temperatures can be observed. As expected, the

[5] Note that the currents are very similar and can hardly be distinguished in the plot.

temperatures rise during the conducting phase of the transistor and fall during its blocking phase. The small temperature changes do not have a significant influence on the currents.

In another experiment, a failure of the system (short circuit) is simulated. In this extreme situation, the voltage v_{ds} across the transistors remains at U_0, while the current is no longer limited by I_0. Instead, the current through the transistor is only limited by Equation (1), namely $K(v_{gs} - V_T)^2$. Since this leads to extremely high currents, the temperatures will rise quickly to significant higher values. This in turn will influence the value of K and V_T, which will eventually lead to decreasing currents.

The simulation run is shown in Figure 26(b), using the same parameters as in the previous run. The first period is shown in detail in Figure 27, using a higher synchronization rate of $\tau_s = 0.1\,\mu s$.

As expected, the temperatures rise quickly. While the hottest segment heats up by nearly $70\,K$ within $1\,ms$, the coolest segment increases only by $20\,K$. Due to this large temperature spread, the currents begin to deviate, as can be seen in the upper plot. Here, the lowest of the four current curves corresponds to the hottest segment in the semiconductor.

7 Conclusions

We have explained in this report how to model and simulate the electrothermal behavior in a simple case study of a MOSFET transistor. We have studied the evolution of the electrical and thermal outputs of the transistor when it is driven by a periodic square wave voltage.

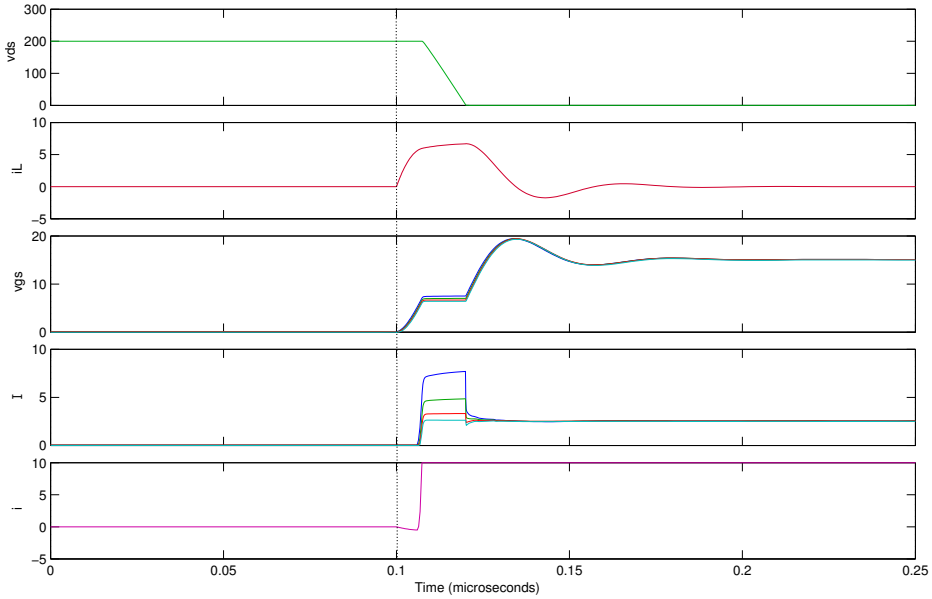
We have used the tool MATLAB/SIMULINK for simulating the electrical behavior and the tool CASTEM for simulating the thermal behavior. We have simulated the behaviors under normal conditions and under stress (repeated short-circuits). We have observed the coupling between the thermal subsystem and the electrical subsystem in the case of stress conditions.

In a next step, we will compare the results of the present simulation with experimental results observed in the SATIE laboratory on a real implemented system.

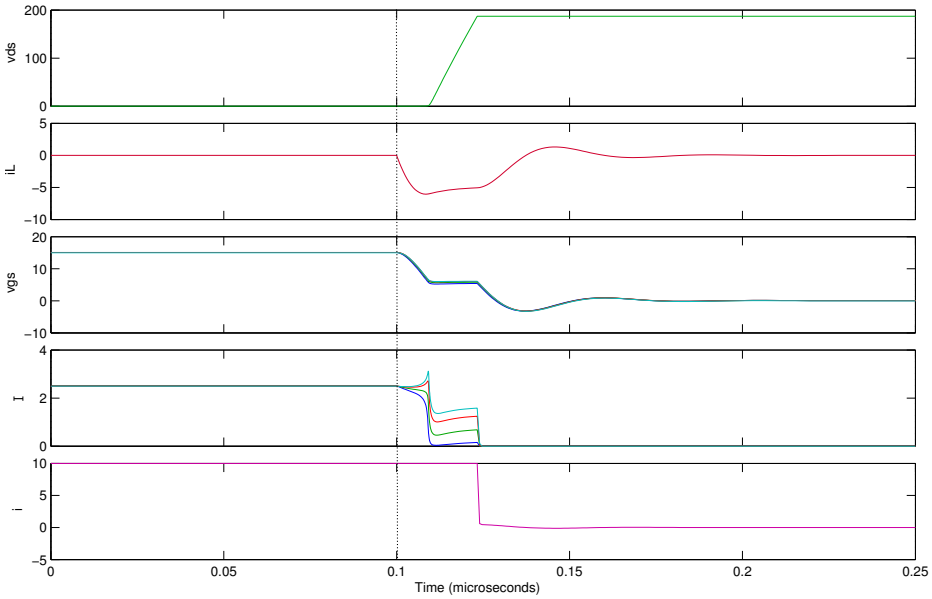
References

1. Castem. http://www-cast3m.cea.fr.
2. M. Arab, S. Lefebvre, Z. Khatir, and S. Bontemps. Investigations on ageing of IGBT transistors under repetitive short-circuits operations. In *Proceedings of PCIM*, 2008.
3. M. Bonnet and A. Frangi. *Analyse des solides déformables par la méthode des Éléments finis.* Les editions de l'Ecole Polytechnique, 2006.
4. M. Ciappa. Selected failure mechanisms of modern power modules. *Microelectronics Reliability*, 42(4-5):653 – 667, 2002.
5. S. Lefebvre, Z. Khatir, and F. St-Eve. Behavior of single chip IGBT devices under repetitive short-circuit conditions. *IEEE Trans. on Electron Devices*, 52(2), 2 2005.

6. S. Wünsche. Simulator coupling for electro-thermal simulation of integrated circuits. In *International Workshop on Thermal Investigations of ICs and Microstructures*, pages 89–93, 1996.

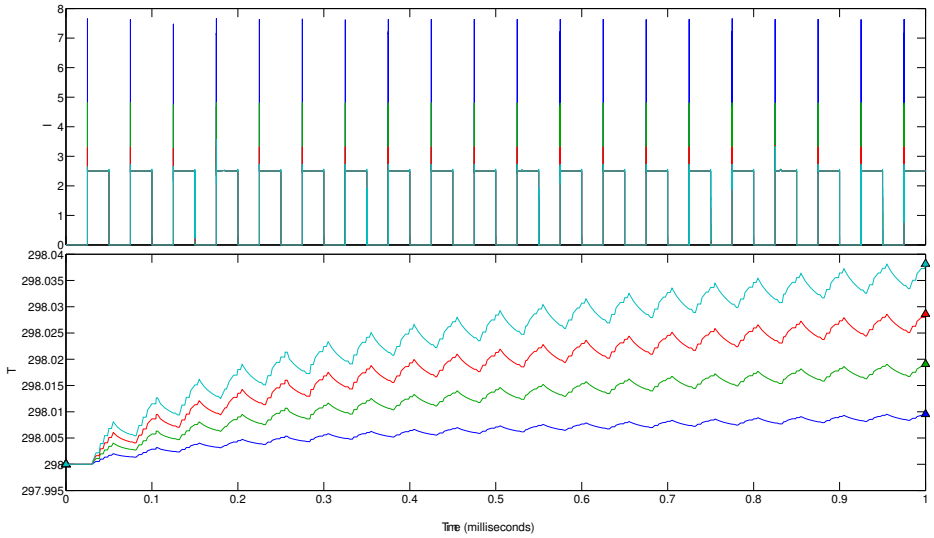


(a) Rising edge of V_{GS}

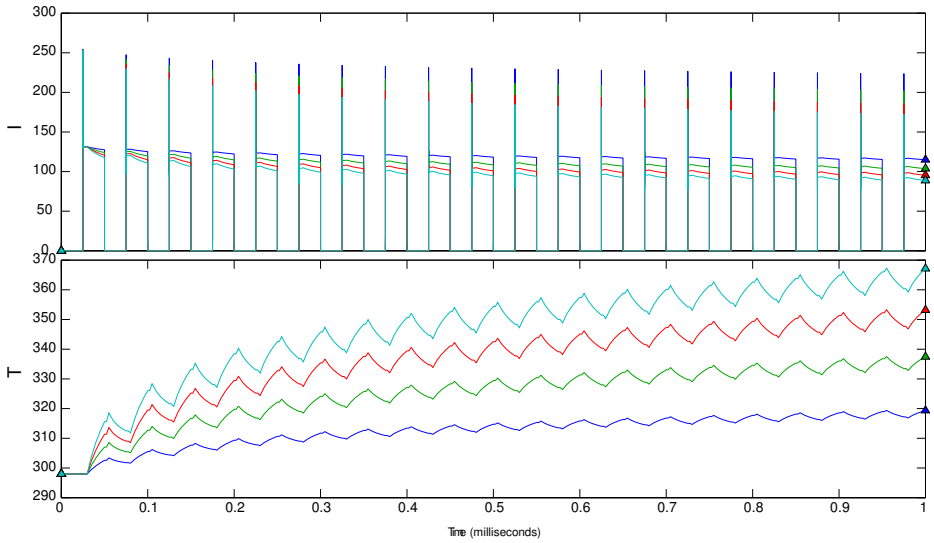


(b) Falling edge of V_{GS}

Fig. 25. Phase changes of V_{GS}



(a) Normal operation



(b) Saturation

Fig. 26. Coupled simulation

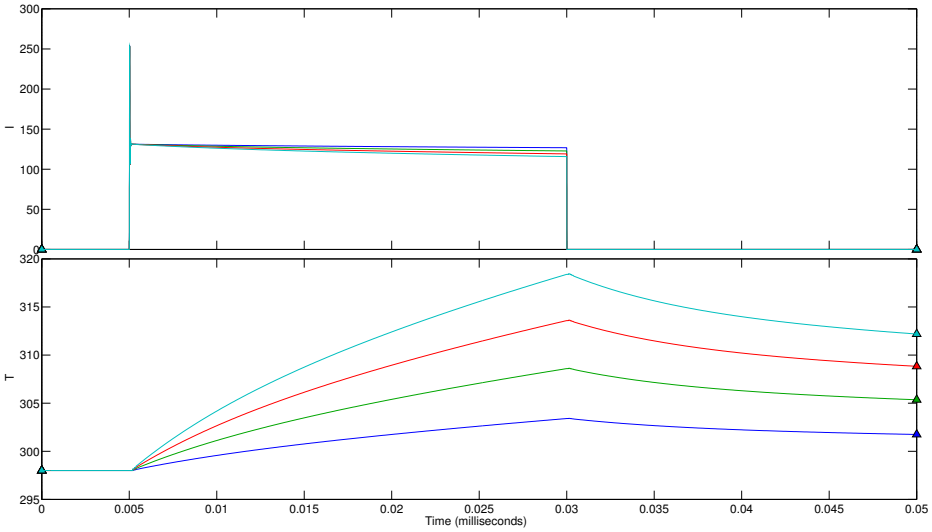


Fig. 27. Detail of Figure 26