Projet VALMEM

Sujet: « Vérification des circuits mémoires »

- Document 3 -

Traduction Automatique de Descriptions VHDL en description TA du programme vhdl2ta

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Dans ce document nous allons présenter les expérimentations qui a étaient faites jusqu'à présent sur quelques modèles VHDL. On commence d'abord par décrire les tests unitaires qu'on a fait sur des modèles simples (une affectation, un processus) avant de passer au tests des modèles plus complexes. On rappelle que notre but est de tester l'architecture de la mémoie SPSMALL.

1. Tests unitaires :

Dans cette section, nous allons présenter les résultats de tests obtenus sur les descriptions hytech et uppaal générées par le programme respectivement à partir des modèles VHDL suivants :

- la description ass1.vhd qui contient une affectation simple d'un signal.
- la description prc1.vhd qui contient un seul processus.

Pour chaque modèle VHDL, on va se restreindre de présenter sa description en hytech. On note que les descriptions en uppaal sont décrite d'une manière similaire aux descriptions en hytech.

Evidemment, les résultats de tests obtenus sur les descriptions en hytech sont les mêmes que ceux obtenus en utilisant les descriptions en uppaal.

1.1. La description exp1.hy

Elle est générée avec les options :

- version éclatées: non.
- optimisation des gardes simples : non/oui.
- optimisation de la figure : non/oui.

Le programme VHDL et la description hytech associée sont donnés ci-après :

```
//*          programme vhdl ass1.vhd          *//
//-------------------------------------------//
-- Entity Declaration
ENTITY n_xor IS
  PORT (
         s  : out   BIT;
         e_1 : in    BIT;
         e_2 : in    BIT
  );
END n_xor;

-- Architecture Declaration
ARCHITECTURE RTL OF n_xor IS

BEGIN
  s <= not (e_1 xor e_2);
END;

//*          declalration des variables          *//
//-----------------------------------------------//
var   t,
      x_s   : clock;
      e_2,
      e_1,
      s
      : discrete;
      delta0_s, delta1_s      : parameter;

//* les automates qui definissent le signal s *//
//-------------------------------------------//
automaton Ass_s
synclabs: e_1_up, e_1_down, e_2_up, e_2_down, s_up, s_down;
initially l_f_s ;
loc l_x0_s : while x_s <= delta0_s wait {}
      when  e_1 = 0  sync e_1_down goto l_x0_s;
      when  e_1 = 1  sync e_1_up goto l_x0_s;
      when e_1 = 1-0   & e_2 = 0 sync e_1_down do{ x_s'=0 } goto l_x1_s;
      when e_1 = 1-1   & e_2 = 1 sync e_1_up do{ x_s'=0 } goto l_x1_s;
      when  e_2 = 0  sync e_2_down goto l_x0_s;
      when  e_2 = 1  sync e_2_up goto l_x0_s;
      when e_2 = 1-0   & e_1 = 0 sync e_2_down do{ x_s'=0 } goto l_x1_s;
      when e_2 = 1-1   & e_1 = 1 sync e_2_up do{ x_s'=0 } goto l_x1_s;
      when  x_s = delta0_s sync s_down do {s' = 0} goto l_f_s;
loc l_x1_s : while x_s <= delta1_s wait {}
      when  e_1 = 0  sync e_1_down goto l_x1_s;
      when  e_1 = 1  sync e_1_up goto l_x1_s;
      when e_1 = 1-0   & e_2 = 1 sync e_1_down do{ x_s'=0 } goto l_x0_s;
      when e_1 = 1-1   & e_2 = 0 sync e_1_up do{ x_s'=0 } goto l_x0_s;
      when  e_2 = 0  sync e_2_down goto l_x1_s;
      when  e_2 = 1  sync e_2_up goto l_x1_s;
      when e_2 = 1-0   & e_1 = 1 sync e_2_down do{ x_s'=0 } goto l_x0_s;
```

```
      when e_2 = 1-1   & e_1 = 0 sync e_2_up do{ x_s'=0 } goto l_x0_s;
      when  x_s = delta1_s sync s_up do {s' = 1} goto l_f_s;

loc l_f_s : while True wait {}
      when  e_1 = 0  sync e_1_down goto l_f_s;
      when  e_1 = 1  sync e_1_up goto l_f_s;
      when e_1 = 1-0   & e_2 = 0 sync e_1_down do{ x_s'=0 } goto l_x1_s;
      when e_1 = 1-0   & e_2 = 1 sync e_1_down do{ x_s'=0 } goto l_x0_s;
      when e_1 = 1-1   & e_2 = 1 sync e_1_up do{ x_s'=0 } goto l_x1_s;
      when e_1 = 1-1   & e_2 = 0 sync e_1_up do{ x_s'=0 } goto l_x0_s;
      when  e_2 = 0  sync e_2_down goto l_f_s;
      when  e_2 = 1  sync e_2_up goto l_f_s;
      when e_2 = 1-0   & e_1 = 0 sync e_2_down do{ x_s'=0 } goto l_x1_s;
      when e_2 = 1-0   & e_1 = 1 sync e_2_down do{ x_s'=0 } goto l_x0_s;
      when e_2 = 1-1   & e_1 = 1 sync e_2_up do{ x_s'=0 } goto l_x1_s;
      when e_2 = 1-1   & e_1 = 0 sync e_2_up do{ x_s'=0 } goto l_x0_s;
end
```

- Résultats d'analyse avec Hytech :

L'analyse de la description hytech a été faite sur plusieurs environnements. Les délais des signaux sont tous égaux à 1. On note aussi que la propriété de stabilité de signal de sortie s, mentionnée ci-dessous, est vérifiée sur le graphe d'accessibilité dans tous les environnements qu'on a fait passer.

– empty (atteign_reg & final_reg), tel que :

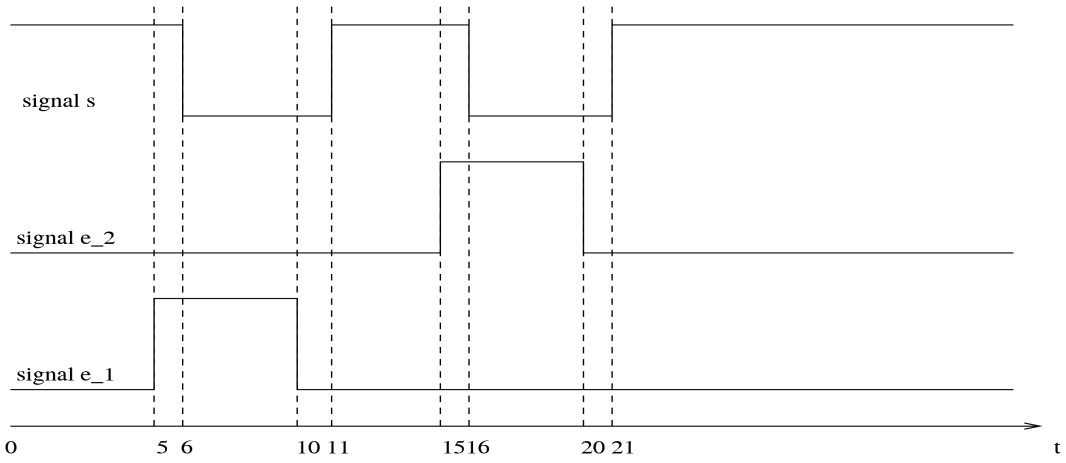
  atteign_reg := reach forward from init_reg endreach;

  final_reg := loc[Ass_s]=l_f_s & ~ ((e_1 = e_2 & s = 1) | (~(e_1 = e_2) & s = 0));

Cette dernière propriété est exprimée dans uppaal par :

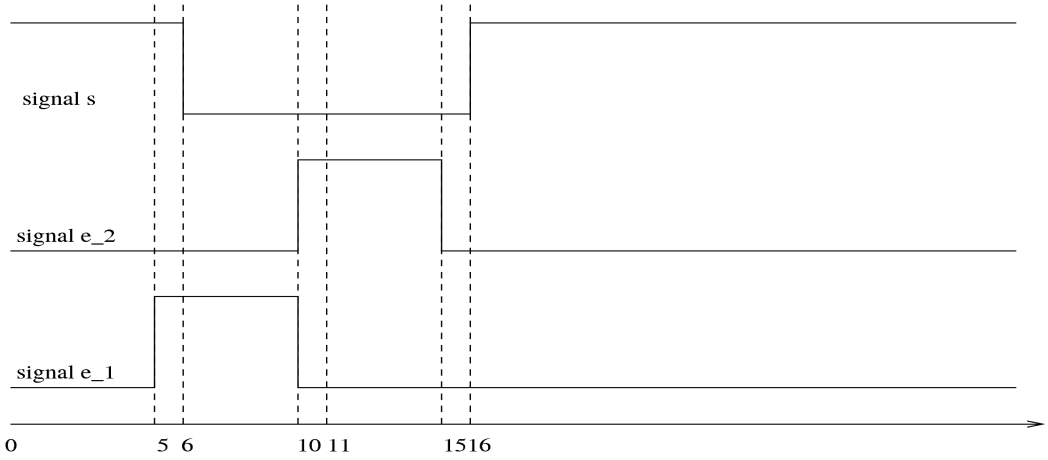
A[] (Ass_s_i1.l_f_s imply s == ((e_1 imply e_2) and (e_2 imply e_1))).

Environnement 1 (t(e1_up) < t(e1_down) < t(e2_up) < t(e2_down):



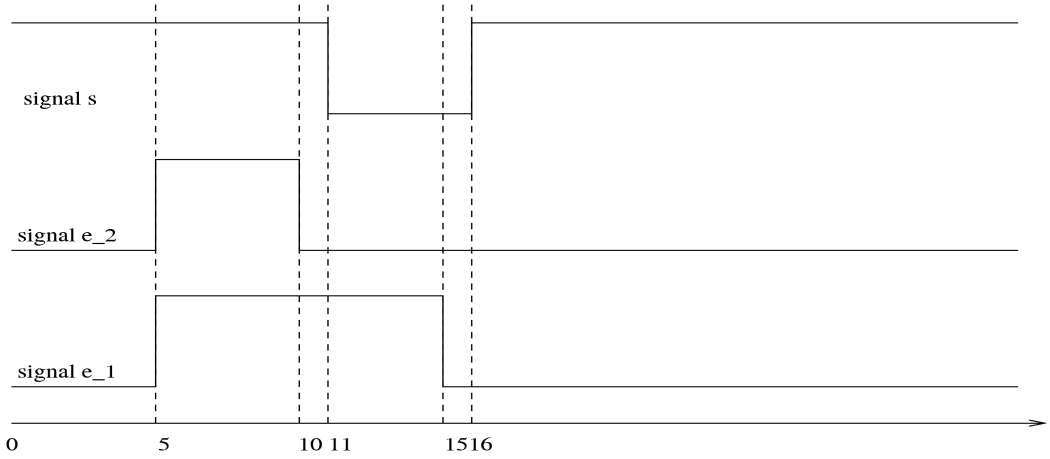

```
Composing automata *
.........Number of iterations required for reachability: 9

atteign:
--------
Location: env_nd_signals_0.l_f_s
     e_1 = 0   & s = 1   & e_2 = 0   & t >= 0   & t <= 5
Location: env_nd_signals_1.l_x0_s
     e_1 = 1   & s = 1   & e_2 = 0   & t <= 6   & t >= 5
Location: env_nd_signals_1.l_f_s
     e_1 = 1   & s = 0   & e_2 = 0   & t >= 6   & t <= 10
Location: env_nd_signals_2.l_x1_s
     e_1 = 0   & s = 0   & e_2 = 0   & t <= 11   & t >= 10
Location: env_nd_signals_2.l_f_s
     e_1 = 0   & s = 1   & e_2 = 0   & t >= 11   & t <= 15
Location: env_nd_signals_3.l_x0_s
     e_1 = 0   & s = 1   & e_2 = 1   & t <= 16   & t >= 15
Location: env_nd_signals_3.l_f_s
     e_1 = 0   & s = 0   & e_2 = 1   & t >= 16   & t <= 20
Location: env_nd_signals_end.l_x1_s
     e_1 = 0   & s = 0   & e_2 = 0   & t >= 20   & t <= 21
Location: env_nd_signals_end.l_f_s
     s = 1   & e_1 = 0   & e_2 = 0   & t >= 21
```

Environnement 2 (t(e1_up) < t(e1_down) = t(e2_up) < t(e2_down):



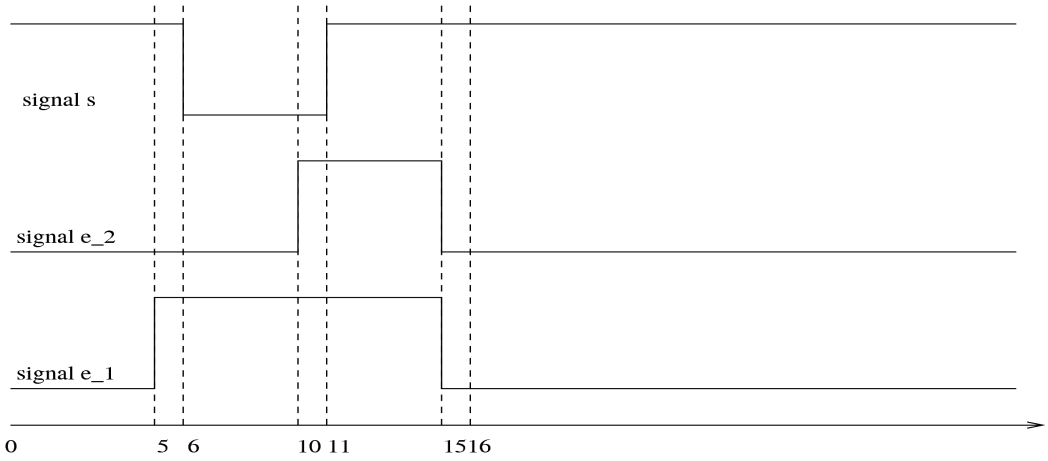

```
Composing automata *
........Number of iterations required for reachability: 8

atteign:
--------
Location: env_e_1_0.env_e_2_0.l_f_s
     e_1 = 0   & s = 1   & e_2 = 0   & t >= 0   & t <= 5
Location: env_e_1_1.env_e_2_0.l_x0_s
     e_1 = 1   & s = 1   & e_2 = 0   & t <= 6   & t >= 5
Location: env_e_1_1.env_e_2_0.l_f_s
     e_1 = 1   & s = 0   & e_2 = 0   & t >= 6   & t <= 10

Location: env_e_1_end.env_e_2_0.l_x1_s
     t = 10   & s = 0   & e_2 = 0   & e_1 = 0
Location: env_e_1_1.env_e_2_1.l_x1_s
     t = 10   & s = 0   & e_2 = 1   & e_1 = 1

Location: env_e_1_end.env_e_2_1.l_x0_s
     e_1 = 0   & s = 0   & e_2 = 1   & t <= 11   & t >= 10
Location: env_e_1_end.env_e_2_1.l_f_s
     e_1 = 0   & s = 0   & e_2 = 1   & t >= 11   & t <= 15
Location: env_e_1_end.env_e_2_end.l_x1_s
     e_1 = 0   & s = 0   & e_2 = 0   & t >= 15   & t <= 16
Location: env_e_1_end.env_e_2_end.l_f_s
     s = 1   & e_1 = 0   & e_2 = 0   & t >= 16
```

Environnement 3 (t(e1_up) = t(e2_up) < t(e2_down) < t(e1_down):



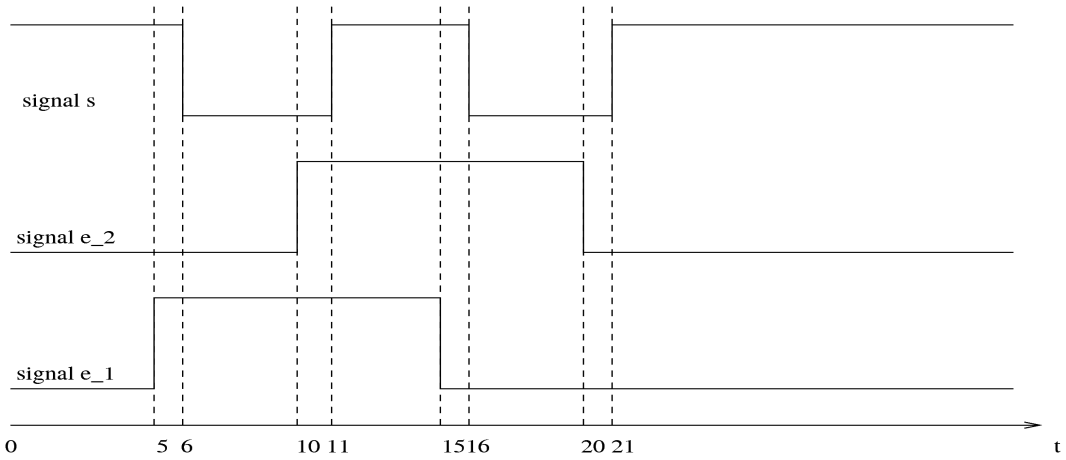

```
Composing automata *
........Number of iterations required for reachability: 8

atteign:
--------
Location: env_e_1_0.env_e_2_0.l_f_s
     e_1 = 0   & s = 1   & e_2 = 0   & t >= 0   & t <= 5

Location: env_e_1_0.env_e_2_1.l_x0_s
     t = 5   & s = 1   & e_2 = 1   & e_1 = 0
Location: env_e_1_1.env_e_2_0.l_x0_s
     t = 5   & s = 1   & e_2 = 0   & e_1 = 1

Location: env_e_1_1.env_e_2_1.l_x1_s
     e_1 = 1   & s = 1   & e_2 = 1   & t <= 6   & t >= 5
Location: env_e_1_1.env_e_2_1.l_f_s
     e_1 = 1   & s = 1   & e_2 = 1   & t >= 6   & t <= 10
Location: env_e_1_1.env_e_2_end.l_x0_s
     e_1 = 1   & s = 1   & e_2 = 0   & t <= 11   & t >= 10
Location: env_e_1_1.env_e_2_end.l_f_s
     e_1 = 1   & s = 0   & e_2 = 0   & t >= 11   & t <= 15
Location: env_e_1_end.env_e_2_end.l_x1_s
     e_1 = 0   & s = 0   & e_2 = 0   & t >= 15   & t <= 16
Location: env_e_1_end.env_e_2_end.l_f_s
     s = 1   & e_1 = 0   & e_2 = 0   & t >= 16
```

Environnement 4 (t(e1_up) < t(e2_up) < t(e2_down) = t(e1_down):



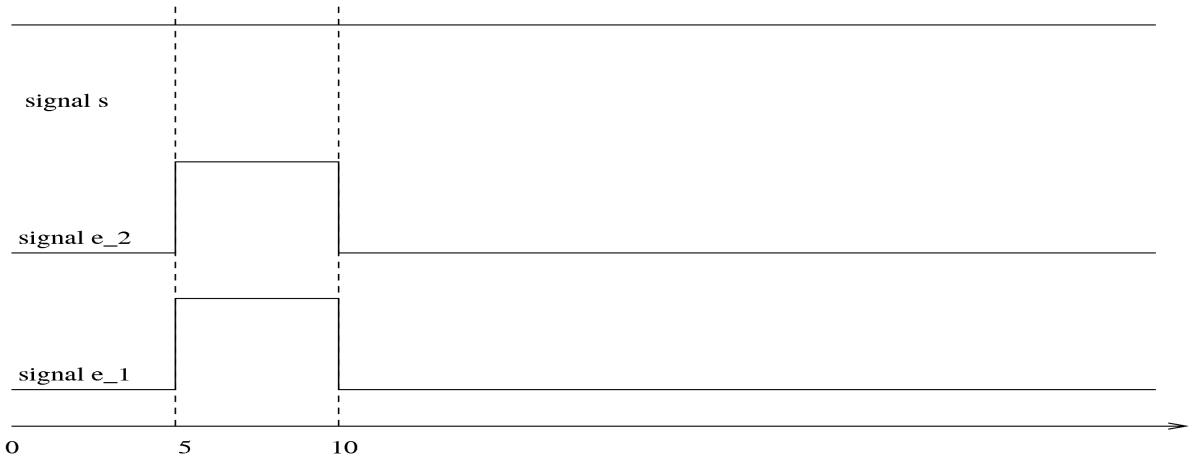

```
Composing automata *
........Number of iterations required for reachability: 8

atteign:
--------
Location: env_e_1_0.env_e_2_0.l_f_s
     e_1 = 0   & s = 1   & e_2 = 0   & t >= 0   & t <= 5
Location: env_e_1_1.env_e_2_0.l_x0_s
     e_1 = 1   & s = 1   & e_2 = 0   & t <= 6   & t >= 5
Location: env_e_1_1.env_e_2_0.l_f_s
     e_1 = 1   & s = 0   & e_2 = 0   & t >= 6   & t <= 10
Location: env_e_1_1.env_e_2_1.l_x1_s
     e_1 = 1   & s = 0   & e_2 = 1   & t <= 11   & t >= 10
Location: env_e_1_1.env_e_2_1.l_f_s
     e_1 = 1   & s = 1   & e_2 = 1   & t >= 11   & t <= 15

Location: env_e_1_end.env_e_2_1.l_x0_s
     t = 15   & s = 1   & e_2 = 1   & e_1 = 0
Location: env_e_1_1.env_e_2_end.l_x0_s
     t = 15   & s = 1   & e_2 = 0   & e_1 = 1

Location: env_e_1_end.env_e_2_end.l_x1_s
     e_1 = 0   & s = 1   & e_2 = 0   & t >= 15   & t <= 16
Location: env_e_1_end.env_e_2_end.l_f_s
     s = 1   & e_1 = 0   & e_2 = 0   & t >= 16
```

Environnement 5 (t(e1_up) < t(e2_up) < t(e1_down) < t(e2_down):




```
Composing automata *
.........Number of iterations required for reachability: 9

atteign:
--------
Location: env_nd_signals_0.l_f_s
     e_1 = 0   & s = 1   & e_2 = 0   & t >= 0   & t <= 5
Location: env_nd_signals_1.l_x0_s
     e_1 = 1   & s = 1   & e_2 = 0   & t <= 6   & t >= 5
Location: env_nd_signals_1.l_f_s
     e_1 = 1   & s = 0   & e_2 = 0   & t >= 6   & t <= 10
Location: env_nd_signals_2.l_x1_s
     e_1 = 1   & s = 0   & e_2 = 1   & t <= 11   & t >= 10
Location: env_nd_signals_2.l_f_s
     e_1 = 1   & s = 1   & e_2 = 1   & t >= 11   & t <= 15
Location: env_nd_signals_3.l_x0_s
     e_1 = 0   & s = 1   & e_2 = 1   & t <= 16   & t >= 15
Location: env_nd_signals_3.l_f_s
     e_1 = 0   & s = 0   & e_2 = 1   & t >= 16   & t <= 20
Location: env_nd_signals_end.l_x1_s
     e_1 = 0   & s = 0   & e_2 = 0   & t >= 20   & t <= 21
Location: env_nd_signals_end.l_f_s
     s = 1   & e_1 = 0   & e_2 = 0   & t >= 21
```

Environnement 6 (t(e1_up) = t(e2_up) < t(e1_down) = t(e2_down):




```
Composing automata *
.......Number of iterations required for reachability: 7

atteign:
--------
Location: env_e_1_0.env_e_2_0.l_f_s
     e_1 = 0   & s = 1   & e_2 = 0   & t >= 0   & t <= 5

Location: env_e_1_1.env_e_2_0.l_x0_s
     t = 5   & s = 1   & e_2 = 0   & e_1 = 1
Location: env_e_1_0.env_e_2_1.l_x0_s
     t = 5   & s = 1   & e_2 = 1   & e_1 = 0

Location: env_e_1_1.env_e_2_1.l_x1_s
     e_1 = 1   & s = 1   & e_2 = 1   & t <= 6   & t >= 5
Location: env_e_1_1.env_e_2_1.l_f_s
     e_1 = 1   & s = 1   & e_2 = 1   & t >= 6   & t <= 10

Location: env_e_1_end.env_e_2_1.l_x0_s
     t = 10   & s = 1   & e_2 = 1   & e_1 = 0
Location: env_e_1_1.env_e_2_end.l_x0_s
     t = 10   & s = 1   & e_2 = 0   & e_1 = 1

Location: env_e_1_end.env_e_2_end.l_x1_s
     e_1 = 0   & s = 1   & e_2 = 0   & t >= 10   & t <= 11

Location: env_e_1_end.env_e_2_end.l_f_s
     s = 1   & e_1 = 0   & e_2 = 0   & t >= 11
```

1.2. La description prc1.hy

Elle est générée avec les options :

version éclatées: non.
optimisation des gardes simples : oui
optimisation de la figure : non/oui

Comme une remarque, on avait testé auparavant la description générée sans optimisation des gardes. Les résultats de tests sont les mêmes.

```
//*          programme vhdl ass1.vhd          *//
//-------------------------------------------//
-- Entity Declaration
ENTITY n_xor IS
  PORT (
         s  : out   BIT;
         e_1 : in    BIT;
         e_2 : in    BIT
  );
END n_xor;

-- Architecture Declaration
ARCHITECTURE RTL OF n_xor IS

BEGIN
  s <= not (e_1 xor e_2);
END;

La description hytech est la suivante :

//*          programme vhdl ass1.vhd          *//
//-------------------------------------------//
-- Entity Declaration
ENTITY Prc1 IS
  PORT (
         a : in    BIT;
         b : in    BIT;
         d : in    BIT;
         e : in    BIT;
         s : out   BIT
  );
END Prc1;

-- Architecture Declaration
ARCHITECTURE RTL OF Prc1 IS
BEGIN
Pr1: PROCESS (a, b, d, e)
BEGIN
  IF a = '1' THEN
    s <= d;
  ELSIF b = '1' THEN
    s <= e;
  END IF;
END PROCESS;
END;

//*          declalration des variables          *//
//-----------------------------------------------//
var
      t,
```

```
      x_pr1 : clock;

      e,
      d,
      b,
      a,
      s
      : discrete;

      delta0_1_pr1, delta1_1_pr1,
      delta0_2_pr1, delta1_2_pr1,
      delta0_pr1, delta1_pr1  : parameter;

//*    l'automate qui définissent le signal s   *//
//---------------------------------------------//
automaton P_pr1

synclabs: a_up, a_down, b_up, b_down, d_up, d_down, e_up, e_down, s_up, s_down ;
initially l_s_P_pr1;

loc l_x0_P_pr1 : while x_pr1 <= delta0_pr1  wait {}

-- les transitions sensibles aux changements des signaux d'entrees e1, ... ,
e4 :
-- cas B1 = 1 :
      when  a = 1 & d = 0  sync d_down goto l_x0_P_pr1;
      when a = 1 & d = 1-1 sync d_up do{ x_pr1'=0 } goto l_x1_P_pr1;
      when  a = 1 sync e_down goto l_x0_P_pr1;
      when  a = 1 sync e_up goto l_x0_P_pr1;

-- cas B1 = 0 & B2 = 1 :
      when  a = 0 & b = 1 sync d_down goto l_x0_P_pr1;
      when  a = 0 & b = 1 sync d_up goto l_x0_P_pr1;
      when  a = 0 & b = 1 & e = 0  sync e_down goto l_x0_P_pr1;
      when a = 0 & b = 1 & e = 1-1 sync e_up do{ x_pr1'=0 } goto l_x1_P_pr1;

-- les transitions synchronisés avec le signal de sortie s :
      when a = 1 &  x_pr1 = delta0_1_pr1 sync s_down do {s' = 0} goto l_f_P_pr1;
      when a = 0 & b = 1 &  x_pr1 = delta0_2_pr1 sync s_down do {s' = 0} goto
l_f_P_pr1;

-- les transitions sensibles aux changements des signaux B1, ... , B2 :
-- cas B1 = 1 :
      when a = 1 sync b_down goto l_x0_P_pr1;
      when a = 1 sync b_up goto l_x0_P_pr1;
      when a = 1 & b = 1   & d = 0  & e = 0 sync a_down goto l_x0_P_pr1;
      when a = 1 & b = 1   & d = 0  & e = 1 sync a_down do{ x_pr1'=0 } goto
l_x1_P_pr1;
      when a = 1 & b = 0 sync a_down goto l_s_P_pr1;

-- cas B1 = 0 & B2 = 1 :
      when a = 0 & b = 1   & e = 0  & d = 0 sync a_up goto l_x0_P_pr1;
      when a = 0 & b = 1   & e = 0  & d = 1 sync a_up do{ x_pr1'=0 } goto
l_x1_P_pr1;
      when a = 0 & b = 1 sync b_down goto l_s_P_pr1;

loc l_x1_P_pr1 : while x_pr1 <= delta1_pr1  wait {}

-- les transitions sensibles aux changements des signaux d'entrees e1, ... ,
e4 :
-- cas B1 = 1 :
      when  a = 1 & d = 1  sync d_up goto l_x1_P_pr1;
```

```
      when a = 1 & d = 1-0 sync d_down do{ x_pr1'=0 } goto l_x0_P_pr1;
      when  a = 1 sync e_down goto l_x1_P_pr1;
      when  a = 1 sync e_up goto l_x1_P_pr1;

-- cas B1 = 0 & B2 = 1 :
      when  a = 0 & b = 1 sync d_down goto l_x1_P_pr1;
      when  a = 0 & b = 1 sync d_up goto l_x1_P_pr1;
      when  a = 0 & b = 1 & e = 1  sync e_up goto l_x1_P_pr1;
      when a = 0 & b = 1 & e = 1-0 sync e_down do{ x_pr1'=0 } goto l_x0_P_pr1;

-- les transitions synchronisés avec le signal de sortie s :
      when a = 1 &  x_pr1 = delta1_1_pr1 sync s_up do {s' = 1} goto l_f_P_pr1;
      when a = 0 & b = 1 &  x_pr1 = delta1_2_pr1 sync s_up do {s' = 1} goto
l_f_P_pr1;

-- les transitions sensibles aux changements des signaux B1, ... , B2 :
-- cas B1 = 1 :
      when a = 1 sync b_down goto l_x1_P_pr1;
      when a = 1 sync b_up goto l_x1_P_pr1;
      when a = 1 & b = 1   & d = 1  & e = 1 sync a_down goto l_x1_P_pr1;
      when a = 1 & b = 1   & d = 1  & e = 0 sync a_down do{ x_pr1'=0 } goto
l_x0_P_pr1;
      when a = 1 & b = 0 sync a_down goto l_s_P_pr1;

-- cas B1 = 0 & B2 = 1 :
      when a = 0 & b = 1   & e = 1  & d = 1 sync a_up goto l_x1_P_pr1;
      when a = 0 & b = 1   & e = 1  & d = 0 sync a_up do{ x_pr1'=0 } goto
l_x0_P_pr1;
      when a = 0 & b = 1 sync b_down goto l_s_P_pr1;

loc l_f_P_pr1 : while True wait {}

-- les transitions sensibles aux changements des signaux d'entrees e1, ... , e4
du process :
-- cas B1 = 1 :
      when  a = 1 & d = 0  sync d_down goto l_f_P_pr1;
      when  a = 1 & d = 1  sync d_up goto l_f_P_pr1;
      when a = 1 & d = 1-0 sync d_down do{ x_pr1'=0 } goto l_x0_P_pr1;
      when a = 1 & d = 1-1 sync d_up do{ x_pr1'=0 } goto l_x1_P_pr1;
      when  a = 1 sync e_down goto l_f_P_pr1;
      when  a = 1 sync e_up goto l_f_P_pr1;

-- cas B1 = 0 & B2 = 1 :
      when  a = 0 & b = 1 sync d_down goto l_f_P_pr1;
      when  a = 0 & b = 1 sync d_up goto l_f_P_pr1;
      when  a = 0 & b = 1 & e = 0  sync e_down goto l_f_P_pr1;
      when  a = 0 & b = 1 & e = 1  sync e_up goto l_f_P_pr1;
      when a = 0 & b = 1 & e = 1-0 sync e_down do{ x_pr1'=0 } goto l_x0_P_pr1;
      when a = 0 & b = 1 & e = 1-1 sync e_up do{ x_pr1'=0 } goto l_x1_P_pr1;

-- les transitions sensibles aux changements des signaux B1, ... , B2 :
-- cas B1 = 1 :
      when a = 1 sync b_down goto l_f_P_pr1;
      when a = 1 sync b_up goto l_f_P_pr1;
      when a = 1 & b = 1   & d = 0  & e = 0 sync a_down goto l_f_P_pr1;
      when a = 1 & b = 1   & d = 1  & e = 1 sync a_down goto l_f_P_pr1;
      when a = 1 & b = 1   & d = 0  & e = 1 sync a_down do{ x_pr1'=0 } goto
l_x1_P_pr1;
      when a = 1 & b = 1   & d = 1  & e = 0 sync a_down do{ x_pr1'=0 } goto
l_x0_P_pr1;
      when a = 1 & b = 0 sync a_down goto l_s_P_pr1;
```

```
-- cas B1 = 0 & B2 = 1 :
      when a = 0 & b = 1   & e = 0  & d = 0 sync a_up goto l_f_P_pr1;
      when a = 0 & b = 1   & e = 1  & d = 1 sync a_up goto l_f_P_pr1;
      when a = 0 & b = 1   & e = 0  & d = 1 sync a_up do{ x_pr1'=0 } goto
l_x1_P_pr1;
      when a = 0 & b = 1   & e = 1  & d = 0 sync a_up do{ x_pr1'=0 } goto
l_x0_P_pr1;
      when a = 0 & b = 1 sync b_down goto l_s_P_pr1;

loc l_s_P_pr1 : while True wait {}

-- les transitions sensibles aux changements des signaux d'entrees e1, ... , e4
du process :
      when  True  sync d_down goto l_s_P_pr1;
      when  True  sync d_up goto l_s_P_pr1;
      when  True  sync e_down goto l_s_P_pr1;
      when  True  sync e_up goto l_s_P_pr1;

-- les transitions sensibles aux changements des signaux B1, ... , B2 du process
:
      when s = 0   & d = 0 sync a_up goto l_f_P_pr1;
      when s = 1   & d = 1 sync a_up goto l_f_P_pr1;
      when s = 0   & d = 1 sync a_up do{ x_pr1'=0 } goto l_x1_P_pr1;
      when s = 1   & d = 0 sync a_up do{ x_pr1'=0 } goto l_x0_P_pr1;
      when s = 0   & e = 0 sync b_up goto l_f_P_pr1;
      when s = 1   & e = 1 sync b_up goto l_f_P_pr1;
      when s = 0   & e = 1 sync b_up do{ x_pr1'=0 } goto l_x1_P_pr1;
      when s = 1   & e = 0 sync b_up do{ x_pr1'=0 } goto l_x0_P_pr1;

end
```

- Analyse de la description prc1.hy :

L'analyse de la description hytech a été faite sur plusieurs environnements. Les délais des signaux sont tous égaux à 1. On note aussi que la propriété de stabilité de signal de sortie s, mentionnée ci-dessous, est vérifiée sur le graphe d'atteignabilité dans tous les environnements qu'on a passé.

- empty(atteign_reg & final_reg), tel que :

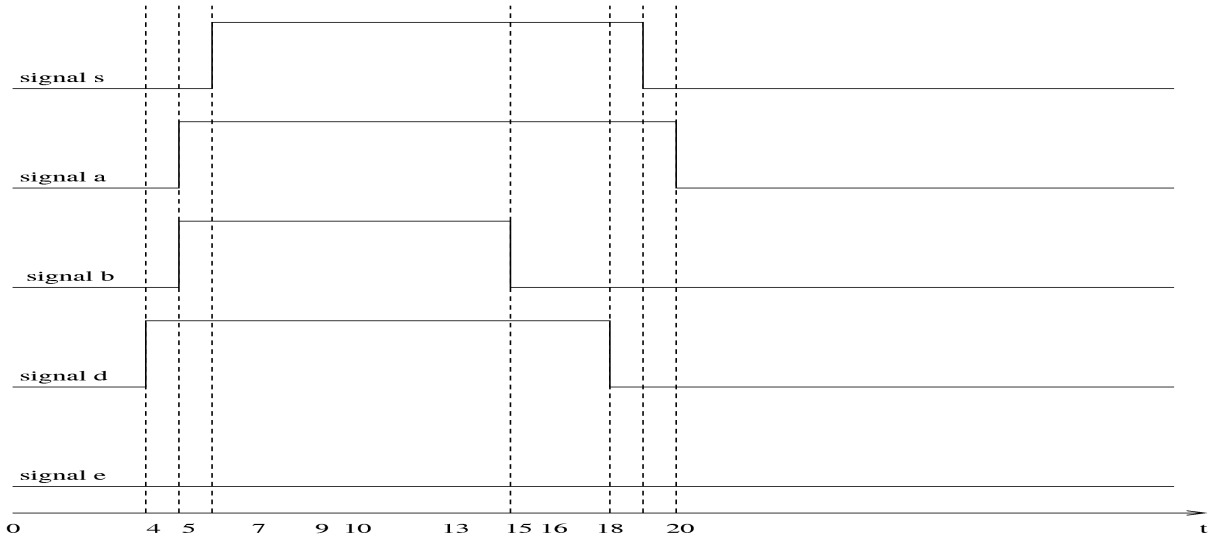
  atteign_reg := reach forward from init_reg endreach;

  final_reg := (loc[P_pr1]=l_f_P_pr1 & ~ ((a = 1 & s = d) | (a = 0 & b = 1 & s = e))) ;

  Cette dernière propriété est exprimée dans uppaal par la formule suivante :

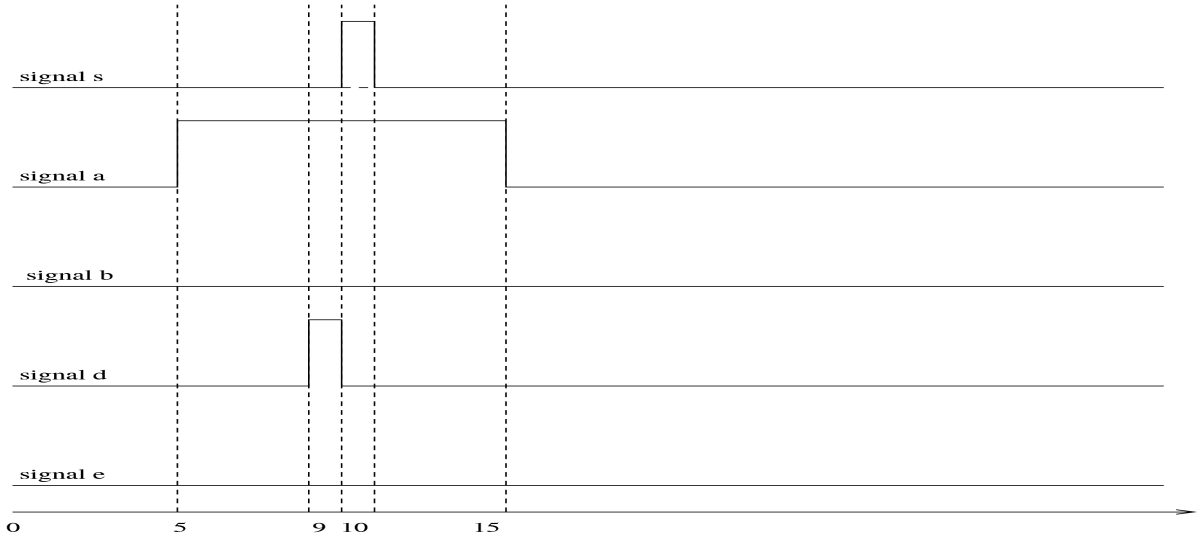
  A[] (P_pr1_i1.l_f_P_pr1 imply ((a == 1 and s == d) or (a == 0 and b == 1 and s == e))).

Environnement 0.1 (t(a_up) = t(b_up) < t(b_down) < t(a_down):



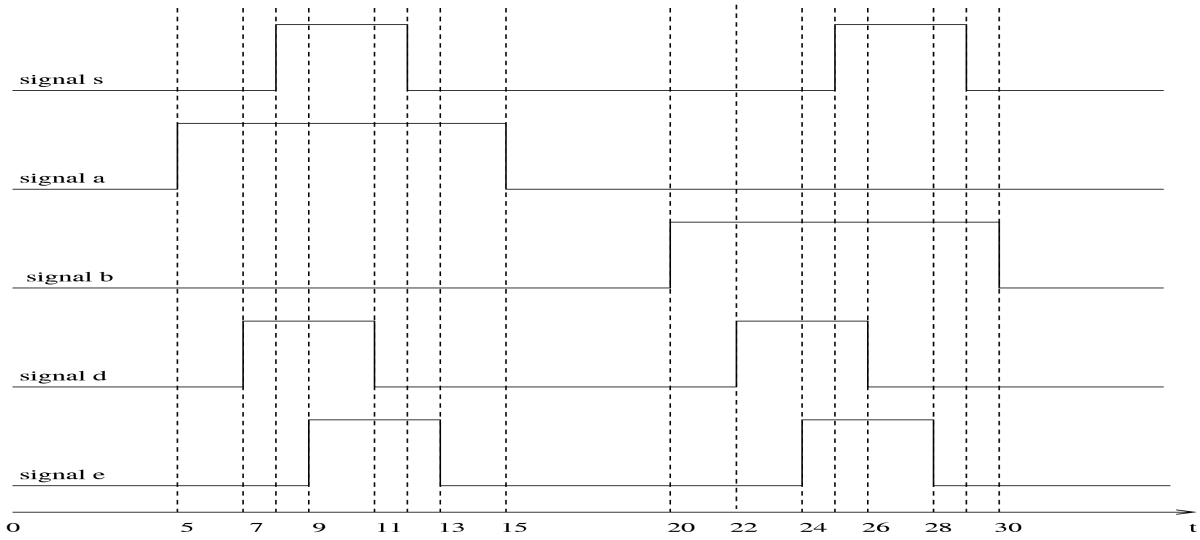

```
Composing automata ***
.........Number of iterations required for reachability: 9

atteign:
--------
Location: env_a_0.env_b_0.env_nd_signals_0.l_s_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 0   & t <= 4
Location: env_a_0.env_b_0.env_nd_signals_1.l_s_P_pr1
     a = 0   & s = 0   & e = 0   & d = 1   & b = 0   & t >= 4   & t <= 5

Location: env_a_0.env_b_1.env_nd_signals_1.l_f_P_pr1
     t = 5   & s = 0   & e = 0   & d = 1   & b = 1   & a = 0

Location: env_a_1.env_b_0.env_nd_signals_1.l_x1_P_pr1
     t = 5   & s = 0   & e = 0   & d = 1   & b = 0   & a = 1
Location: env_a_0.env_b_1.env_nd_signals_1.l_x1_P_pr1
     t = 5   & s = 0   & e = 0   & d = 1   & b = 1   & a = 0

Location: env_a_1.env_b_1.env_nd_signals_1.l_x1_P_pr1
     a = 1   & s = 0   & e = 0   & d = 1   & b = 1   & t <= 6   & t >= 5
Location: env_a_1.env_b_1.env_nd_signals_1.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 1   & t >= 6   & t <= 15
Location: env_a_1.env_b_end.env_nd_signals_1.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 0   & t >= 15   & t <= 18
Location: env_a_1.env_b_end.env_nd_signals_end.l_x0_P_pr1
     a = 1   & s = 1   & e = 0   & d = 0   & b = 0   & t <= 19   & t >= 18
Location: env_a_1.env_b_end.env_nd_signals_end.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 19   & t <= 20
Location: env_a_end.env_b_end.env_nd_signals_end.l_s_P_pr1
     s = 0   & a = 0   & e = 0   & d = 0   & b = 0   & t >= 20
```

Environnement 0.2 (t(a_up) < t(a_down) :



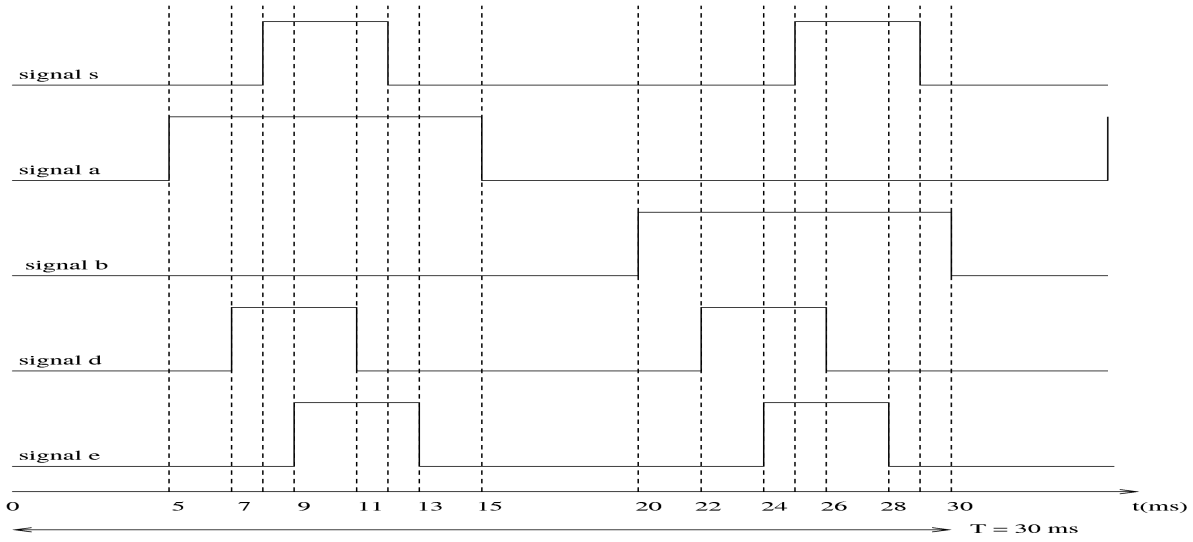

```
Composing automata ***
......Number of iterations required for reachability: 6

atteign:
--------
Location: env_nd_signals_0.l_s_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 0   & t <= 5
Location: env_nd_signals_1.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 5   & t <= 9
Location: env_nd_signals_2.l_x1_P_pr1
     a = 1   & s = 0   & e = 0   & d = 1   & b = 0   & t >= 9   & t <= 10
Location: env_nd_signals_2.l_f_P_pr1
     t = 10   & s = 1   & e = 0   & d = 1   & b = 0   & a = 1

Location: env_nd_signals_3.l_x0_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 0   & t <= 11   & t >= 10
|
     a = 1   & s = 1   & e = 0   & d = 0   & b = 0   & t <= 11   & t >= 10

Location: env_nd_signals_3.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 11   & t <= 15
Location: env_nd_signals_end.l_s_P_pr1
     s = 0   & a = 0   & e = 0   & d = 0   & b = 0   & t >= 15
```

Environnement 1.1 (t(a_up) < t(a_down) < t(b_up) < t(b_down):



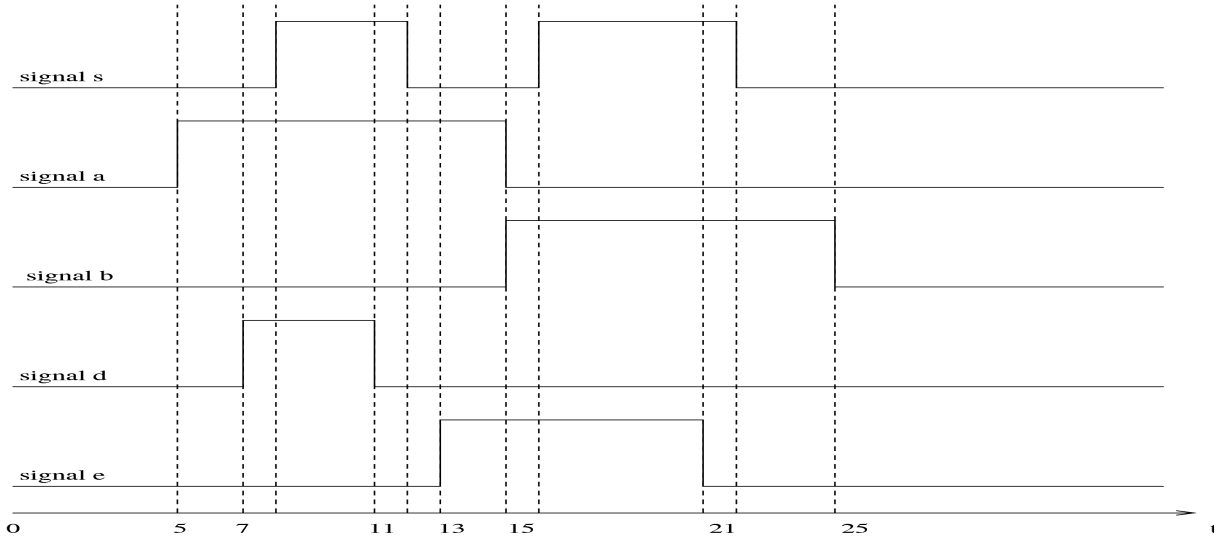

```
Composing automata ***
.....................Number of iterations required for reachability: 17

atteign:
------
Location: env_nd_signals_0.l_s_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 0   & t <= 5
Location: env_nd_signals_1.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 5   & t <= 7
Location: env_nd_signals_2.l_x1_P_pr1
     a = 1   & s = 0   & e = 0   & d = 1   & b = 0   & t <= 8   & t >= 7
Location: env_nd_signals_2.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 0   & t >= 8   & t <= 9
Location: env_nd_signals_3.l_f_P_pr1
     a = 1   & s = 1   & e = 1   & d = 1   & b = 0   & t >= 9   & t <= 11
Location: env_nd_signals_4.l_x0_P_pr1
     a = 1   & s = 1   & e = 1   & d = 0   & b = 0   & t <= 12   & t >= 11
Location: env_nd_signals_4.l_f_P_pr1
     a = 1   & s = 0   & e = 1   & d = 0   & b = 0   & t >= 12   & t <= 13
Location: env_nd_signals_5.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 13   & t <= 15
Location: env_nd_signals_6.l_s_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 15   & t <= 20
Location: env_nd_signals_7.l_f_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 1   & t >= 20   & t <= 22
Location: env_nd_signals_8.l_f_P_pr1
     a = 0   & s = 0   & e = 0   & d = 1   & b = 1   & t >= 22   & t <= 24
Location: env_nd_signals_9.l_x1_P_pr1
     a = 0   & s = 0   & e = 1   & d = 1   & b = 1   & t <= 25   & t >= 24
Location: env_nd_signals_9.l_f_P_pr1
     a = 0   & s = 1   & e = 1   & d = 1   & b = 1   & t >= 25   & t <= 26
Location: env_nd_signals_10.l_f_P_pr1
     a = 0   & s = 1   & e = 1   & d = 0   & b = 1   & t >= 26   & t <= 28
Location: env_nd_signals_11.l_x0_P_pr1
     a = 0   & s = 1   & e = 0   & d = 0   & b = 1   & t <= 29   & t >= 28
Location: env_nd_signals_11.l_f_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 1   & t >= 29   & t <= 30
Location: env_nd_signals_end.l_s_P_pr1
     s = 0   & a = 0   & e = 0   & d = 0   & b = 0   & t >= 30
```

Environnement 1.2 (t(a_up) < t(a_down) < t(b_up) < t(b_down) (cas périodique):



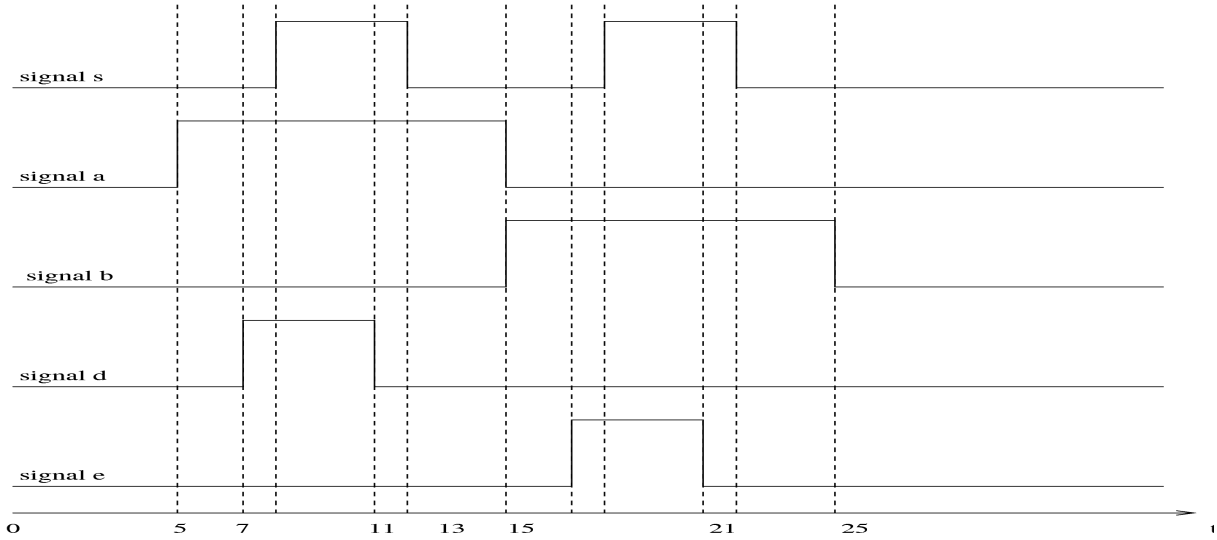

```
Composing automata ***
.................Number of iterations required for reachability: 16

atteign:
--------
Location: env_nd_signals_0.l_s_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 0   & t <= 5
Location: env_nd_signals_1.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 5   & t <= 7
Location: env_nd_signals_2.l_x1_P_pr1
     a = 1   & s = 0   & e = 0   & d = 1   & b = 0   & t <= 8   & t >= 7
Location: env_nd_signals_2.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 0   & t >= 8   & t <= 9
Location: env_nd_signals_3.l_f_P_pr1
     a = 1   & s = 1   & e = 1   & d = 1   & b = 0   & t >= 9   & t <= 11
Location: env_nd_signals_4.l_x0_P_pr1
     a = 1   & s = 1   & e = 1   & d = 0   & b = 0   & t <= 12   & t >= 11
Location: env_nd_signals_4.l_f_P_pr1
     a = 1   & s = 0   & e = 1   & d = 0   & b = 0   & t >= 12   & t <= 13
Location: env_nd_signals_5.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 13   & t <= 15
Location: env_nd_signals_6.l_s_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 15   & t <= 20
Location: env_nd_signals_7.l_f_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 1   & t >= 20   & t <= 22
Location: env_nd_signals_8.l_f_P_pr1
     a = 0   & s = 0   & e = 0   & d = 1   & b = 1   & t >= 22   & t <= 24
Location: env_nd_signals_9.l_x1_P_pr1
     a = 0   & s = 0   & e = 1   & d = 1   & b = 1   & t <= 25   & t >= 24
Location: env_nd_signals_9.l_f_P_pr1
     a = 0   & s = 1   & e = 1   & d = 1   & b = 1   & t >= 25   & t <= 26
Location: env_nd_signals_10.l_f_P_pr1
     a = 0   & s = 1   & e = 1   & d = 0   & b = 1   & t >= 26   & t <= 28
Location: env_nd_signals_11.l_x0_P_pr1
     a = 0   & s = 1   & e = 0   & d = 0   & b = 1   & t <= 29   & t >= 28
Location: env_nd_signals_11.l_f_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 1   & t >= 29   & t <= 30
```

Environnement 1.3 (t(a_up) < t(a_down) = t(b_up) < t(b_down):



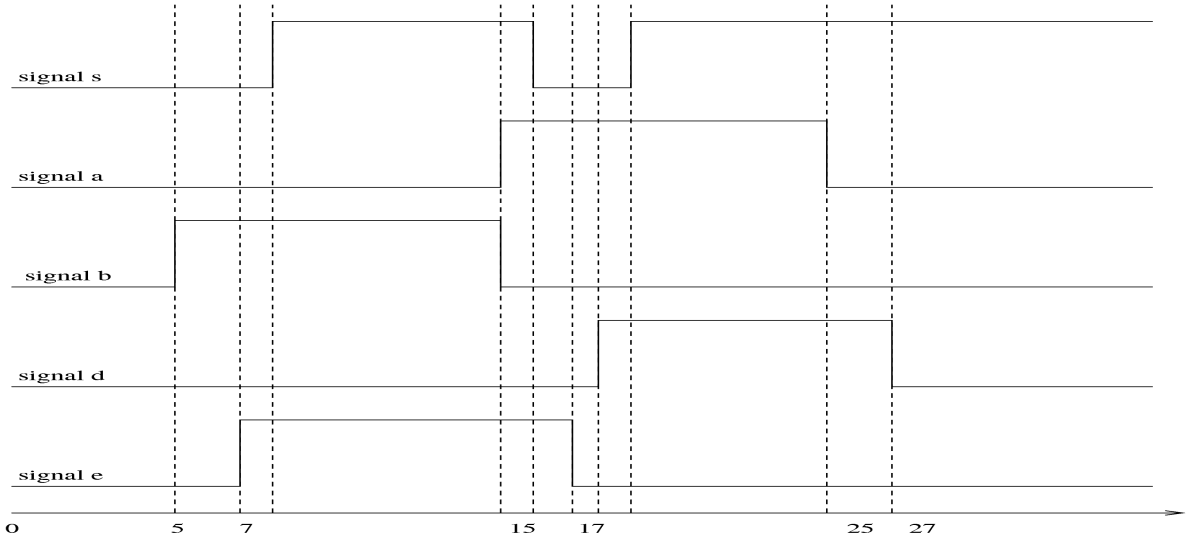

```
Composing automata ***
.............Number of iterations required for reachability: 13

atteign:
--------
Location: env_a_0.env_b_0.env_nd_signals_0.l_s_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 0   & t <= 5
Location: env_a_1.env_b_0.env_nd_signals_0.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 5   & t <= 7
Location: env_a_1.env_b_0.env_nd_signals_1.l_x1_P_pr1
     a = 1   & s = 0   & e = 0   & d = 1   & b = 0   & t <= 8   & t >= 7
Location: env_a_1.env_b_0.env_nd_signals_1.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 0   & t >= 8   & t <= 11

Location: env_a_1.env_b_0.env_nd_signals_2.l_x0_P_pr1
     a = 1   & s = 1   & e = 0   & d = 0   & b = 0   & t <= 12   & t >= 11
Location: env_a_1.env_b_0.env_nd_signals_2.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 12   & t <= 13
Location: env_a_1.env_b_0.env_nd_signals_3.l_f_P_pr1
     a = 1   & s = 0   & e = 1   & d = 0   & b = 0   & t >= 13   & t <= 15

Location: env_a_1.env_b_1.env_nd_signals_3.l_f_P_pr1
     t = 15   & s = 0   & e = 1   & d = 0   & b = 1   & a = 1
Location: env_a_end.env_b_0.env_nd_signals_3.l_s_P_pr1
     t = 15   & s = 0   & e = 1   & d = 0   & b = 0   & a = 0

Location: env_a_end.env_b_1.env_nd_signals_3.l_x1_P_pr1
     a = 0   & s = 0   & e = 1   & d = 0   & b = 1   & t <= 16   & t >= 15
Location: env_a_end.env_b_1.env_nd_signals_3.l_f_P_pr1
     a = 0   & s = 1   & e = 1   & d = 0   & b = 1   & t >= 16   & t <= 21
Location: env_a_end.env_b_1.env_nd_signals_end.l_x0_P_pr1
     a = 0   & s = 1   & e = 0   & d = 0   & b = 1   & t <= 22   & t >= 21
Location: env_a_end.env_b_1.env_nd_signals_end.l_f_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 1   & t >= 22   & t <= 25
Location: env_a_end.env_b_end.env_nd_signals_end.l_s_P_pr1
     s = 0   & a = 0   & e = 0   & d = 0   & b = 0   & t >= 25
```

Environnement 1.3' (t(a_up) < t(a_down) = t(b_up) < t(b_down):



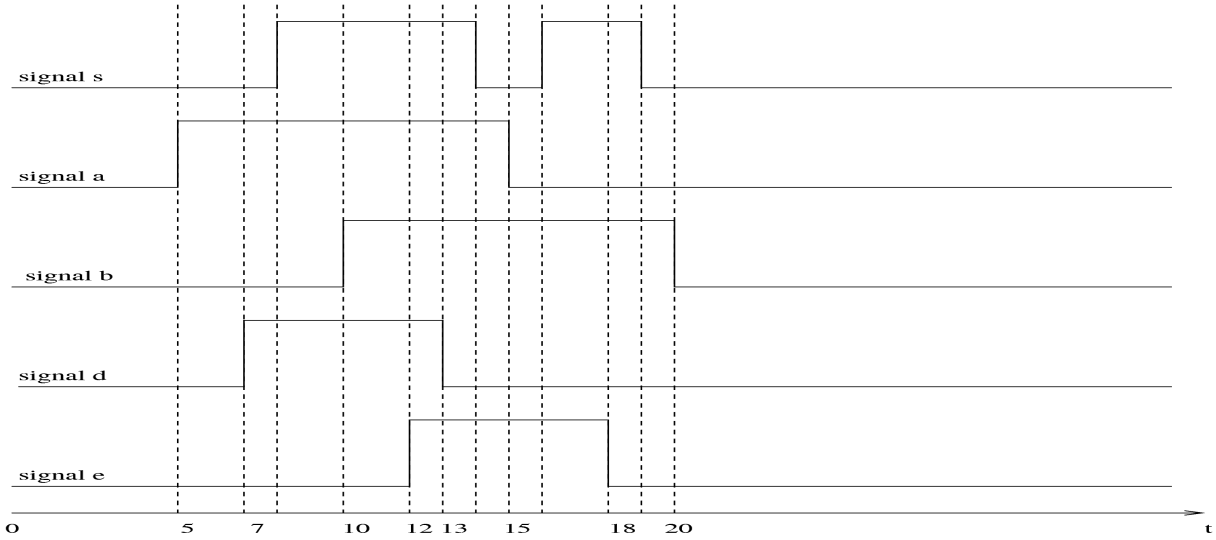

```
Composing automata ***
.............Number of iterations required for reachability: 13

atteign:
--------
Location: env_a_0.env_b_0.env_nd_signals_0.l_s_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 0   & t <= 5
Location: env_a_1.env_b_0.env_nd_signals_0.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 5   & t <= 7
Location: env_a_1.env_b_0.env_nd_signals_1.l_x1_P_pr1
     a = 1   & s = 0   & e = 0   & d = 1   & b = 0   & t <= 8   & t >= 7
Location: env_a_1.env_b_0.env_nd_signals_1.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 0   & t >= 8   & t <= 11
Location: env_a_1.env_b_0.env_nd_signals_2.l_x0_P_pr1
     a = 1   & s = 1   & e = 0   & d = 0   & b = 0   & t <= 12   & t >= 11
Location: env_a_1.env_b_0.env_nd_signals_2.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 12   & t <= 15

Location: env_a_1.env_b_1.env_nd_signals_2.l_f_P_pr1
     t = 15   & s = 0   & e = 0   & d = 0   & b = 1   & a = 1
Location: env_a_end.env_b_0.env_nd_signals_2.l_s_P_pr1
     t = 15   & s = 0   & e = 0   & d = 0   & b = 0   & a = 0

Location: env_a_end.env_b_1.env_nd_signals_2.l_f_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 1   & t >= 15   & t <= 17
Location: env_a_end.env_b_1.env_nd_signals_3.l_x1_P_pr1
     a = 0   & s = 0   & e = 1   & d = 0   & b = 1   & t <= 18   & t >= 17
Location: env_a_end.env_b_1.env_nd_signals_3.l_f_P_pr1
     a = 0   & s = 1   & e = 1   & d = 0   & b = 1   & t >= 18   & t <= 21
Location: env_a_end.env_b_1.env_nd_signals_end.l_x0_P_pr1
     a = 0   & s = 1   & e = 0   & d = 0   & b = 1   & t <= 22   & t >= 21
Location: env_a_end.env_b_1.env_nd_signals_end.l_f_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 1   & t >= 22   & t <= 25
Location: env_a_end.env_b_end.env_nd_signals_end.l_s_P_pr1
     s = 0   & a = 0   & e = 0   & d = 0   & b = 0   & t >= 25
```

Environnement 1.4 (t(b_up) < t(b_down) = t(a_up) < t(a_down):



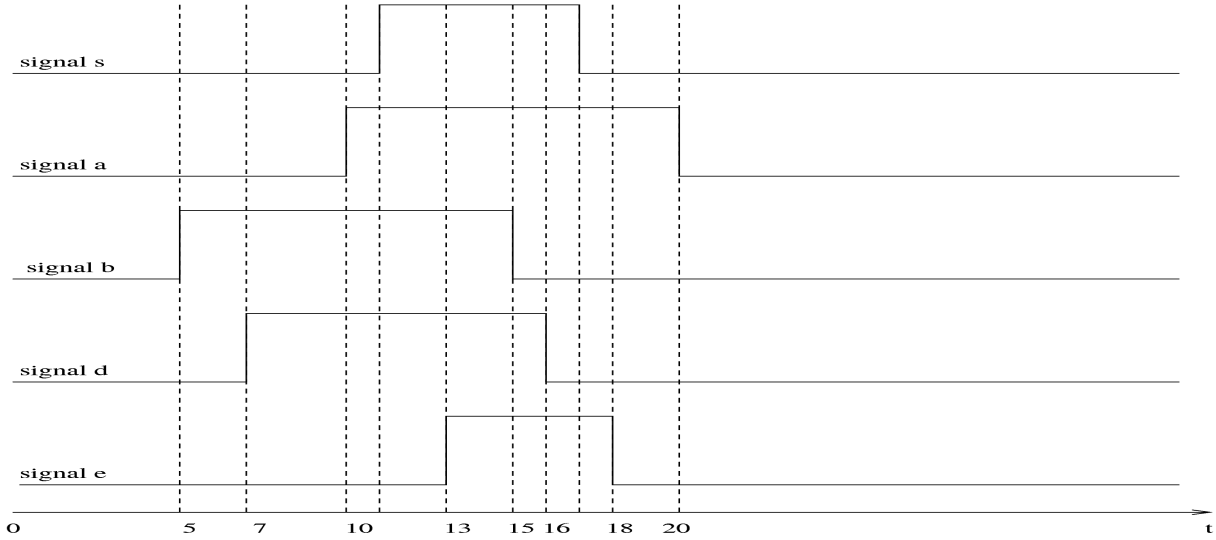

```
Composing automata ***
............Number of iterations required for reachability: 12

atteign:
--------
Location: env_a_0.env_b_0.env_nd_signals_0.l_s_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 0   & t <= 5
Location: env_a_0.env_b_1.env_nd_signals_0.l_f_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 1   & t >= 5   & t <= 7
ocation: env_a_0.env_b_1.env_nd_signals_1.l_x1_P_pr1
     a = 0   & s = 0   & e = 1   & d = 0   & b = 1   & t <= 8   & t >= 7
Location: env_a_0.env_b_1.env_nd_signals_1.l_f_P_pr1
     a = 0   & s = 1   & e = 1   & d = 0   & b = 1   & t >= 8   & t <= 15

Location: env_a_0.env_b_end.env_nd_signals_1.l_s_P_pr1
     t = 15   & s = 1   & e = 1   & d = 0   & b = 0   & a = 0
Location: env_a_1.env_b_1.env_nd_signals_1.l_x0_P_pr1
     t = 15   & s = 1   & e = 1   & d = 0   & b = 1   & a = 1

Location: env_a_1.env_b_end.env_nd_signals_1.l_x0_P_pr1
     a = 1   & s = 1   & e = 1   & d = 0   & b = 0   & t <= 16   & t >= 15
Location: env_a_1.env_b_end.env_nd_signals_1.l_f_P_pr1
     a = 1   & s = 0   & e = 1   & d = 0   & b = 0   & t >= 16   & t <= 17
Location: env_a_1.env_b_end.env_nd_signals_2.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 17   & t <= 18
Location: env_a_1.env_b_end.env_nd_signals_3.l_x1_P_pr1
     a = 1   & s = 0   & e = 0   & d = 1   & b = 0   & t <= 19   & t >= 18
Location: env_a_1.env_b_end.env_nd_signals_3.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 0   & t >= 19   & t <= 25
Location: env_a_end.env_b_end.env_nd_signals_3.l_s_P_pr1
     a = 0   & s = 1   & e = 0   & d = 1   & b = 0   & t >= 25   & t <= 27
Location: env_a_end.env_b_end.env_nd_signals_end.l_s_P_pr1
     s = 1   & a = 0   & e = 0   & d = 0   & b = 0   & t >= 27
```

Environnement 2.1 (t(a_up) < t(b_up) < t(a_down) < t(b_down):



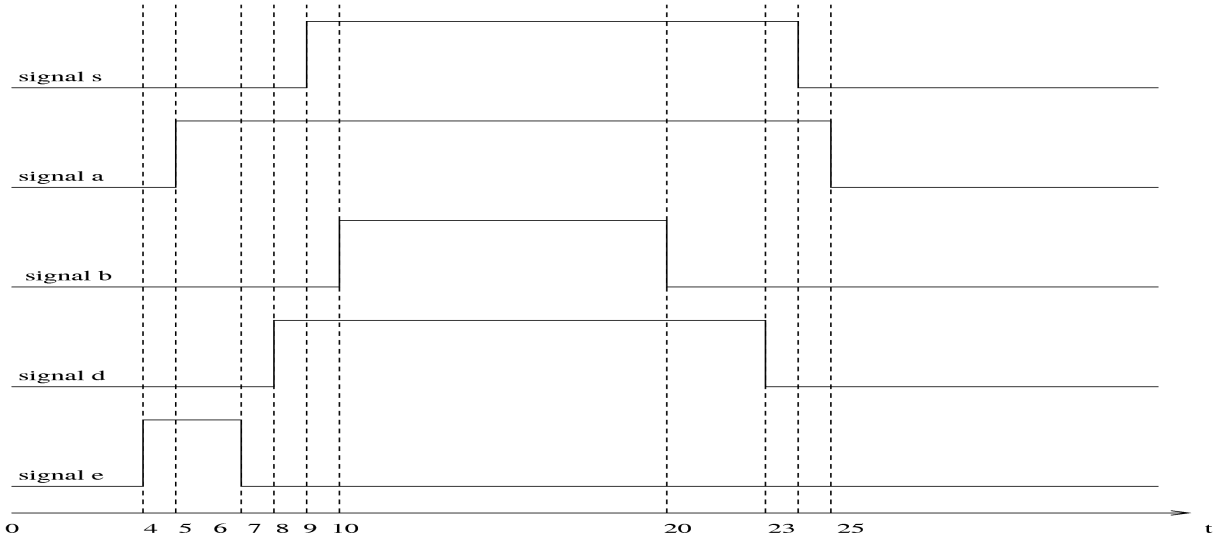

```
Composing automata ***
.............Number of iterations required for reachability: 13

atteign:
--------
Location: env_nd_signals_0.l_s_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 0   & t <= 5
Location: env_nd_signals_1.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 5   & t <= 7
Location: env_nd_signals_2.l_x1_P_pr1
     a = 1   & s = 0   & e = 0   & d = 1   & b = 0   & t <= 8   & t >= 7
Location: env_nd_signals_2.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 0   & t >= 8   & t <= 10
Location: env_nd_signals_3.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 1   & t >= 10   & t <= 12
Location: env_nd_signals_4.l_f_P_pr1
     a = 1   & s = 1   & e = 1   & d = 1   & b = 1   & t >= 12   & t <= 13
Location: env_nd_signals_5.l_x0_P_pr1
     a = 1   & s = 1   & e = 1   & d = 0   & b = 1   & t <= 14   & t >= 13
Location: env_nd_signals_5.l_f_P_pr1
     a = 1   & s = 0   & e = 1   & d = 0   & b = 1   & t >= 14   & t <= 15

Location: env_nd_signals_6.l_x1_P_pr1
     a = 0   & s = 0   & e = 1   & d = 0   & b = 1   & t <= 16   & t >= 15

Location: env_nd_signals_6.l_f_P_pr1
     a = 0   & s = 1   & e = 1   & d = 0   & b = 1   & t >= 16   & t <= 18
Location: env_nd_signals_7.l_x0_P_pr1
     a = 0   & s = 1   & e = 0   & d = 0   & b = 1   & t <= 19   & t >= 18
Location: env_nd_signals_7.l_f_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 1   & t >= 19   & t <= 20
Location: env_nd_signals_end.l_s_P_pr1
     s = 0   & a = 0   & e = 0   & d = 0   & b = 0   & t >= 20
```

Environnement 2.2 (t(b_up) < t(a_up) < t(b_down) < t(a_down):



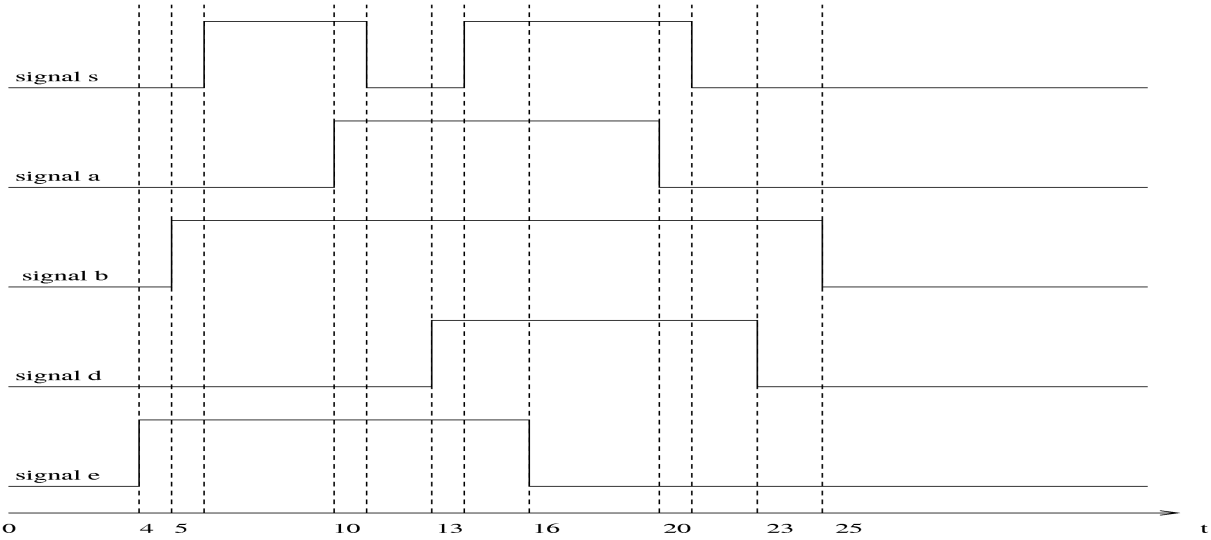

```
Composing automata ***
...........Number of iterations required for reachability: 11

atteign:
--------
Location: env_nd_signals_0.l_s_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 0   & t <= 5
Location: env_nd_signals_1.l_f_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 1   & t >= 5   & t <= 7
Location: env_nd_signals_2.l_f_P_pr1
     a = 0   & s = 0   & e = 0   & d = 1   & b = 1   & t >= 7   & t <= 10
Location: env_nd_signals_3.l_x1_P_pr1
     a = 1   & s = 0   & e = 0   & d = 1   & b = 1   & t <= 11   & t >= 10
Location: env_nd_signals_3.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 1   & t >= 11   & t <= 13
Location: env_nd_signals_4.l_f_P_pr1
     a = 1   & s = 1   & e = 1   & d = 1   & b = 1   & t >= 13   & t <= 15
Location: env_nd_signals_5.l_f_P_pr1
     a = 1   & s = 1   & e = 1   & d = 1   & b = 0   & t >= 15   & t <= 16
Location: env_nd_signals_6.l_x0_P_pr1
     a = 1   & s = 1   & e = 1   & d = 0   & b = 0   & t <= 17   & t >= 16
Location: env_nd_signals_6.l_f_P_pr1
     a = 1   & s = 0   & e = 1   & d = 0   & b = 0   & t >= 17   & t <= 18
Location: env_nd_signals_7.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 18   & t <= 20
Location: env_nd_signals_end.l_s_P_pr1
     s = 0   & a = 0   & e = 0   & d = 0   & b = 0   & t >= 20
```

Environnement 3.1 (t(a_up) < t(b_up) < t(b_down) < t(a_down):



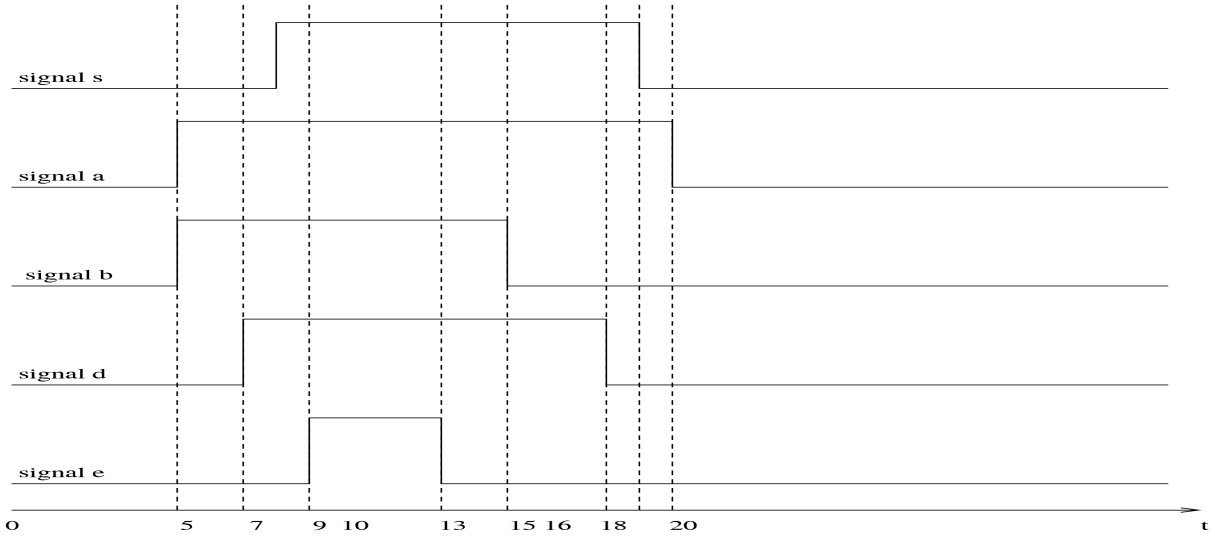

```
Composing automata ***
...........Number of iterations required for reachability: 11

atteign:
--------
Location: env_nd_signals_0.l_s_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 0   & t <= 4
Location: env_nd_signals_1.l_s_P_pr1
     a = 0   & s = 0   & e = 1   & d = 0   & b = 0   & t >= 4   & t <= 5
Location: env_nd_signals_2.l_f_P_pr1
     a = 1   & s = 0   & e = 1   & d = 0   & b = 0   & t >= 5   & t <= 7
Location: env_nd_signals_3.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 7   & t <= 8
Location: env_nd_signals_4.l_x1_P_pr1
     a = 1   & s = 0   & e = 0   & d = 1   & b = 0   & t <= 9   & t >= 8
Location: env_nd_signals_4.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 0   & t >= 9   & t <= 10
Location: env_nd_signals_5.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 1   & t >= 10   & t <= 20
Location: env_nd_signals_6.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 0   & t >= 20   & t <= 23
Location: env_nd_signals_7.l_x0_P_pr1
     a = 1   & s = 1   & e = 0   & d = 0   & b = 0   & t <= 24   & t >= 23
Location: env_nd_signals_7.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 24   & t <= 25
Location: env_nd_signals_end.l_s_P_pr1
     s = 0   & a = 0   & e = 0   & d = 0   & b = 0   & t >= 25
```

Environnement 3.2 (t(b_up) < t(a_up) < t(a_down) < t(b_down):



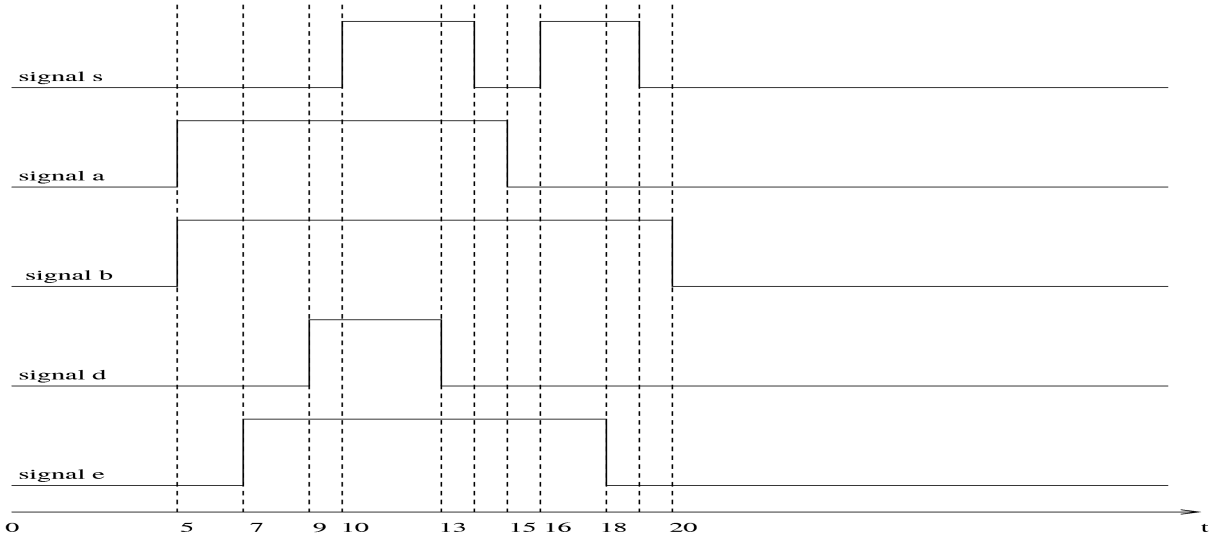

```
Composing automata ***
.............Number of iterations required for reachability: 13

atteign:
--------
Location: env_nd_signals_0.l_s_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 0   & t <= 4
Location: env_nd_signals_1.l_s_P_pr1
     a = 0   & s = 0   & e = 1   & d = 0   & b = 0   & t >= 4   & t <= 5
Location: env_nd_signals_2.l_x1_P_pr1
     a = 0   & s = 0   & e = 1   & d = 0   & b = 1   & t <= 6   & t >= 5
Location: env_nd_signals_2.l_f_P_pr1
     a = 0   & s = 1   & e = 1   & d = 0   & b = 1   & t >= 6   & t <= 10
Location: env_nd_signals_3.l_x0_P_pr1
     a = 1   & s = 1   & e = 1   & d = 0   & b = 1   & t <= 11   & t >= 10
Location: env_nd_signals_3.l_f_P_pr1
     a = 1   & s = 0   & e = 1   & d = 0   & b = 1   & t >= 11   & t <= 13
Location: env_nd_signals_4.l_x1_P_pr1
     a = 1   & s = 0   & e = 1   & d = 1   & b = 1   & t <= 14   & t >= 13
Location: env_nd_signals_4.l_f_P_pr1
     a = 1   & s = 1   & e = 1   & d = 1   & b = 1   & t >= 14   & t <= 16
Location: env_nd_signals_5.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 1   & t >= 16   & t <= 20
Location: env_nd_signals_6.l_x0_P_pr1
     a = 0   & s = 1   & e = 0   & d = 1   & b = 1   & t <= 21   & t >= 20
Location: env_nd_signals_6.l_f_P_pr1
     a = 0   & s = 0   & e = 0   & d = 1   & b = 1   & t >= 21   & t <= 23
Location: env_nd_signals_7.l_f_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 1   & t >= 23   & t <= 25
Location: env_nd_signals_end.l_s_P_pr1
     s = 0   & a = 0   & e = 0   & d = 0   & b = 0   & t >= 25
```

Environnement 3.3 (t(a_up) = t(b_up) < t(b_down) < t(a_down):



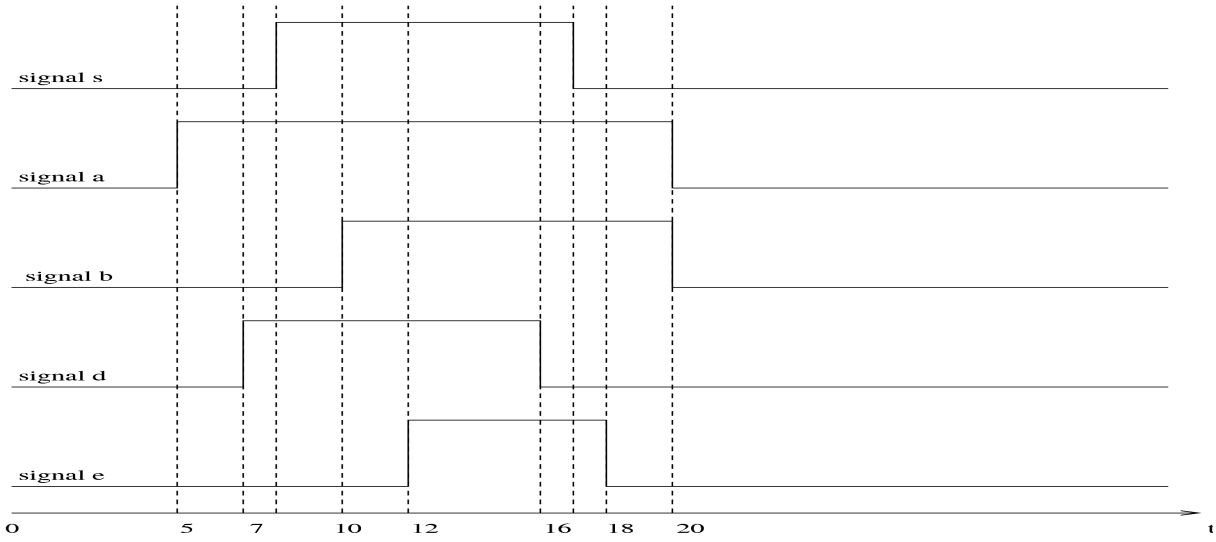

```
Composing automata ***
...........Number of iterations required for reachability: 11

atteign:
--------
Location: env_a_0.env_b_0.env_nd_signals_0.l_s_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 0   & t <= 5

Location: env_a_0.env_b_1.env_nd_signals_0.l_f_P_pr1
     t = 5   & s = 0   & e = 0   & d = 0   & b = 1   & a = 0
Location: env_a_1.env_b_0.env_nd_signals_0.l_f_P_pr1
     t = 5   & s = 0   & e = 0   & d = 0   & b = 0   & a = 1

Location: env_a_1.env_b_1.env_nd_signals_0.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 1   & t >= 5   & t <= 7
Location: env_a_1.env_b_1.env_nd_signals_1.l_x1_P_pr1
     a = 1   & s = 0   & e = 0   & d = 1   & b = 1   & t <= 8   & t >= 7
Location: env_a_1.env_b_1.env_nd_signals_1.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 1   & t >= 8   & t <= 9
Location: env_a_1.env_b_1.env_nd_signals_2.l_f_P_pr1
     a = 1   & s = 1   & e = 1   & d = 1   & b = 1   & t >= 9   & t <= 13
Location: env_a_1.env_b_1.env_nd_signals_3.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 1   & t >= 13   & t <= 15
Location: env_a_1.env_b_end.env_nd_signals_3.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 0   & t >= 15   & t <= 18
Location: env_a_1.env_b_end.env_nd_signals_end.l_x0_P_pr1
     a = 1   & s = 1   & e = 0   & d = 0   & b = 0   & t <= 19   & t >= 18
Location: env_a_1.env_b_end.env_nd_signals_end.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 19   & t <= 20
Location: env_a_end.env_b_end.env_nd_signals_end.l_s_P_pr1
     s = 0   & a = 0   & e = 0   & d = 0   & b = 0   & t >= 20
```

Environnement 3.4 (t(b_up) = t(a_up) < t(a_down) < t(b_down):



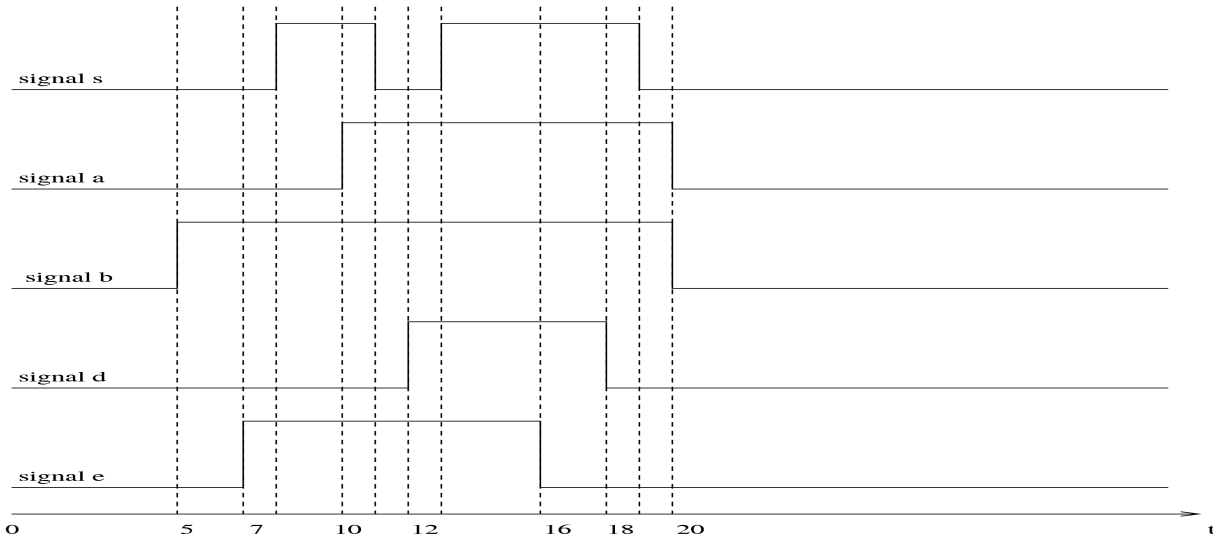

```
Composing automata ***
.............Number of iterations required for reachability: 13

atteign:
--------
Location: env_a_0.env_b_0.env_nd_signals_0.l_s_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 0   & t <= 5

Location: env_a_0.env_b_1.env_nd_signals_0.l_f_P_pr1
     t = 5   & s = 0   & e = 0   & d = 0   & b = 1   & a = 0
Location: env_a_1.env_b_0.env_nd_signals_0.l_f_P_pr1
     t = 5   & s = 0   & e = 0   & d = 0   & b = 0   & a = 1

Location: env_a_1.env_b_1.env_nd_signals_0.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 1   & t >= 5   & t <= 7
Location: env_a_1.env_b_1.env_nd_signals_1.l_f_P_pr1
     a = 1   & s = 0   & e = 1   & d = 0   & b = 1   & t >= 7   & t <= 9
Location: env_a_1.env_b_1.env_nd_signals_2.l_x1_P_pr1
     a = 1   & s = 0   & e = 1   & d = 1   & b = 1   & t <= 10   & t >= 9
Location: env_a_1.env_b_1.env_nd_signals_2.l_f_P_pr1
     a = 1   & s = 1   & e = 1   & d = 1   & b = 1   & t >= 10   & t <= 13
Location: env_a_1.env_b_1.env_nd_signals_3.l_x0_P_pr1
     a = 1   & s = 1   & e = 1   & d = 0   & b = 1   & t <= 14   & t >= 13
Location: env_a_1.env_b_1.env_nd_signals_3.l_f_P_pr1
     a = 1   & s = 0   & e = 1   & d = 0   & b = 1   & t >= 14   & t <= 15
Location: env_a_end.env_b_1.env_nd_signals_3.l_x1_P_pr1
     a = 0   & s = 0   & e = 1   & d = 0   & b = 1   & t <= 16   & t >= 15
Location: env_a_end.env_b_1.env_nd_signals_3.l_f_P_pr1
     a = 0   & s = 1   & e = 1   & d = 0   & b = 1   & t >= 16   & t <= 18
Location: env_a_end.env_b_1.env_nd_signals_end.l_x0_P_pr1
     a = 0   & s = 1   & e = 0   & d = 0   & b = 1   & t <= 19   & t >= 18
Location: env_a_end.env_b_1.env_nd_signals_end.l_f_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 1   & t >= 19   & t <= 20
Location: env_a_end.env_b_end.env_nd_signals_end.l_s_P_pr1
     s = 0   & a = 0   & e = 0   & d = 0   & b = 0   & t >= 20
```

Environnement 3.5 (t(a_up) < t(b_up) < t(b_down) = t(a_down):



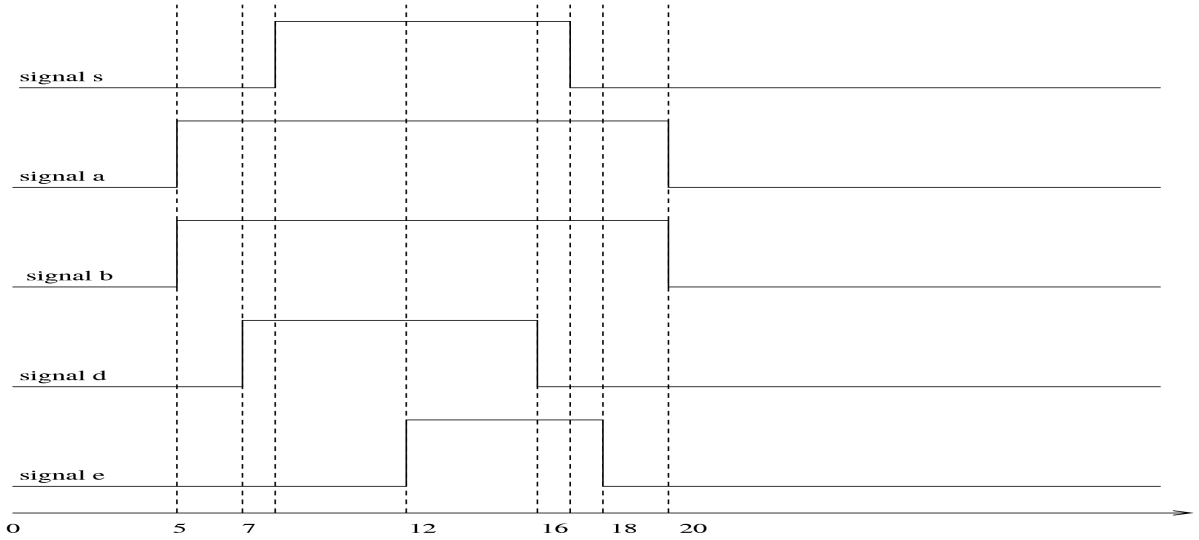

```
Composing automata ***
...........Number of iterations required for reachability: 11

atteign:
--------
Location: env_a_0.env_b_0.env_nd_signals_0.l_s_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 0   & t <= 5
Location: env_a_1.env_b_0.env_nd_signals_0.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 5   & t <= 7
Location: env_a_1.env_b_0.env_nd_signals_1.l_x1_P_pr1
     a = 1   & s = 0   & e = 0   & d = 1   & b = 0   & t <= 8   & t >= 7
Location: env_a_1.env_b_0.env_nd_signals_1.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 0   & t >= 8   & t <= 10
Location: env_a_1.env_b_1.env_nd_signals_1.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 1   & t >= 10   & t <= 12
Location: env_a_1.env_b_1.env_nd_signals_2.l_f_P_pr1
     a = 1   & s = 1   & e = 1   & d = 1   & b = 1   & t >= 12   & t <= 16
Location: env_a_1.env_b_1.env_nd_signals_3.l_x0_P_pr1
     a = 1   & s = 1   & e = 1   & d = 0   & b = 1   & t <= 17   & t >= 16
Location: env_a_1.env_b_1.env_nd_signals_3.l_f_P_pr1
     a = 1   & s = 0   & e = 1   & d = 0   & b = 1   & t >= 17   & t <= 18
Location: env_a_1.env_b_1.env_nd_signals_end.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 1   & t >= 18   & t <= 20

Location: env_a_1.env_b_end.env_nd_signals_end.l_f_P_pr1
     t = 20   & s = 0   & e = 0   & d = 0   & b = 0   & a = 1
Location: env_a_end.env_b_1.env_nd_signals_end.l_f_P_pr1
     t = 20   & s = 0   & e = 0   & d = 0   & b = 1   & a = 0

Location: env_a_end.env_b_end.env_nd_signals_end.l_s_P_pr1
     s = 0   & a = 0   & e = 0   & d = 0   & b = 0   & t >= 20
```

Environnement 3.6 (t(b_up) < t(a_up) < t(a_down) = t(b_down):




```
Composing automata ***
.............Number of iterations required for reachability: 13

atteign:
--------
Location: env_a_0.env_b_0.env_nd_signals_0.l_s_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 0   & t <= 5
Location: env_a_0.env_b_1.env_nd_signals_0.l_f_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 1   & t >= 5   & t <= 7
Location: env_a_0.env_b_1.env_nd_signals_1.l_x1_P_pr1
     a = 0   & s = 0   & e = 1   & d = 0   & b = 1   & t <= 8   & t >= 7
Location: env_a_0.env_b_1.env_nd_signals_1.l_f_P_pr1
     a = 0   & s = 1   & e = 1   & d = 0   & b = 1   & t >= 8   & t <= 10
Location: env_a_1.env_b_1.env_nd_signals_1.l_x0_P_pr1
     a = 1   & s = 1   & e = 1   & d = 0   & b = 1   & t <= 11   & t >= 10
Location: env_a_1.env_b_1.env_nd_signals_1.l_f_P_pr1
     a = 1   & s = 0   & e = 1   & d = 0   & b = 1   & t >= 11   & t <= 12
Location: env_a_1.env_b_1.env_nd_signals_2.l_x1_P_pr1
     a = 1   & s = 0   & e = 1   & d = 1   & b = 1   & t <= 13   & t >= 12
Location: env_a_1.env_b_1.env_nd_signals_2.l_f_P_pr1
     a = 1   & s = 1   & e = 1   & d = 1   & b = 1   & t >= 13   & t <= 16
Location: env_a_1.env_b_1.env_nd_signals_3.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 1   & t >= 16   & t <= 18
Location: env_a_1.env_b_1.env_nd_signals_end.l_x0_P_pr1
     a = 1   & s = 1   & e = 0   & d = 0   & b = 1   & t <= 19   & t >= 18
Location: env_a_1.env_b_1.env_nd_signals_end.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 1   & t >= 19   & t <= 20

Location: env_a_1.env_b_end.env_nd_signals_end.l_f_P_pr1
     t = 20   & s = 0   & e = 0   & d = 0   & b = 0   & a = 1
Location: env_a_end.env_b_1.env_nd_signals_end.l_f_P_pr1
     t = 20   & s = 0   & e = 0   & d = 0   & b = 1   & a = 0

Location: env_a_end.env_b_end.env_nd_signals_end.l_s_P_pr1
     s = 0   & a = 0   & e = 0   & d = 0   & b = 0   & t >= 20
```

Environnement 3.7 (t(a_up) = t(b_up) < t(b_down) = t(a_down):




```
Composing automata ***
...........Number of iterations required for reachability: 11

atteign:
--------
Location: env_a_0.env_b_0.env_nd_signals_0.l_s_P_pr1
     a = 0   & s = 0   & e = 0   & d = 0   & b = 0   & t >= 0   & t <= 5

Location: env_a_1.env_b_0.env_nd_signals_0.l_f_P_pr1
     t = 5   & s = 0   & e = 0   & d = 0   & b = 0   & a = 1
Location: env_a_0.env_b_1.env_nd_signals_0.l_f_P_pr1
     t = 5   & s = 0   & e = 0   & d = 0   & b = 1   & a = 0

Location: env_a_1.env_b_1.env_nd_signals_0.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 1   & t >= 5   & t <= 7
Location: env_a_1.env_b_1.env_nd_signals_1.l_x1_P_pr1
     a = 1   & s = 0   & e = 0   & d = 1   & b = 1   & t <= 8   & t >= 7
Location: env_a_1.env_b_1.env_nd_signals_1.l_f_P_pr1
     a = 1   & s = 1   & e = 0   & d = 1   & b = 1   & t >= 8   & t <= 12
Location: env_a_1.env_b_1.env_nd_signals_2.l_f_P_pr1
     a = 1   & s = 1   & e = 1   & d = 1   & b = 1   & t >= 12   & t <= 16
Location: env_a_1.env_b_1.env_nd_signals_3.l_x0_P_pr1
     a = 1   & s = 1   & e = 1   & d = 0   & b = 1   & t <= 17   & t >= 16
Location: env_a_1.env_b_1.env_nd_signals_3.l_f_P_pr1
     a = 1   & s = 0   & e = 1   & d = 0   & b = 1   & t >= 17   & t <= 18
Location: env_a_1.env_b_1.env_nd_signals_end.l_f_P_pr1
     a = 1   & s = 0   & e = 0   & d = 0   & b = 1   & t >= 18   & t <= 20

Location: env_a_end.env_b_1.env_nd_signals_end.l_f_P_pr1
     t = 20   & s = 0   & e = 0   & d = 0   & b = 1   & a = 0
Location: env_a_1.env_b_end.env_nd_signals_end.l_f_P_pr1
     t = 20   & s = 0   & e = 0   & d = 0   & b = 0   & a = 1

Location: env_a_end.env_b_end.env_nd_signals_end.l_s_P_pr1
     s = 0   & a = 0   & e = 0   & d = 0   & b = 0   & t >= 20
```

2. Tests complexes :

Dans cette deuxième section du document de tests, nous allons présenter les résultats de tests obtenus sur les trois descriptions hytech générées par le programme respectivement à partir des trois modèles VHDL suivants :

- la description exp1.vhd.
- la description LSV.vhd + la description LSV2.vhd
- La description de Pirouz modifiée sp_1x2_md.vhd.

2.1. La description exp1 :

2.1.1. La version non optimisée :

Elle est générée avec les options :

- version éclatée : non.
- optimisation des gardes simples : non.
- optimisation de la figure : non.

La description contient :

- 764 lignes.
- 17 automates (l'automate d'environnement inclus aussi).
- 17 horloges.
- 17 + 2 (i_B) + 2 (B_i) = 21 variables discrètes.
- 32 paramètres.

Le programme VHDL est décrit comme suit :

```
-- Entity Declaration
ENTITY SPSMALL9gp_3x2_nsL IS
  PORT (
         Q_0 : out   BIT;
          CK : in    BIT;
         CSN : in    BIT;
         D_0 : in    BIT
--         vdd : in BIT;
--         gnd : in BIT
  );
END SPSMALL9gp_3x2_nsL;

-- Architecture Declaration
ARCHITECTURE RTL OF SPSMALL9gp_3x2_nsL IS
  SIGNAL v_18_E_net81 : BIT;
  SIGNAL v_18_E_net85 : BIT;
  SIGNAL v_18_E_net83 : BIT;
  SIGNAL v_18_E_data_delay_H : BIT;
  SIGNAL v_17_12_10_net13 : BIT;
  SIGNAL CLK_H : BIT;
  SIGNAL v_18_E_clk_local_L : BIT;
  --SIGNAL v_18_E_clk_local_H : BIT;
  SIGNAL v_17_12_10_net96 : BIT;
  SIGNAL v_17_12_10_ext_cs_H : BIT;
  SIGNAL v_17_12_10_ext_cs_N : BIT;
  SIGNAL v_18_E_data_delay_H_inv : BIT;
  SIGNAL v_17_12_clk_sig_H : BIT;
  SIGNAL v_17_12_10_net41 : BIT;

BEGIN
  v_18_E_net81 <= not (D_0);
  v_18_E_net85 <= not (v_18_E_net81);
  v_18_E_net83 <= not (v_18_E_net85);
  v_18_E_data_delay_H <= not (v_18_E_net83);   -- v4

  v_17_12_10_net13 <= (not (CK) or not (v_17_12_10_ext_cs_N));   -- v8
  v_17_12_clk_sig_H <= not (v_17_12_10_net13);
  v_17_12_10_net41 <= not (v_17_12_clk_sig_H);
  CLK_H <= not (v_17_12_10_net41);
  v_18_E_clk_local_L <= not (CLK_H);     -- v12
```

```
  --v_18_E_clk_local_H <= not (v_18_E_clk_local_L);

  v_17_12_10_net96 <= not (CSN);
  v_17_12_10_ext_cs_H <= not (v_17_12_10_net96);     -- v6

  Q_0 <= v_18_E_data_delay_H_inv;

REG10: PROCESS (CK, v_17_12_10_ext_cs_H) -- v7
BEGIN
  IF CK = '0' THEN
    v_17_12_10_ext_cs_N <= not (v_17_12_10_ext_cs_H);
  END IF;
END PROCESS;

REG12: PROCESS (v_18_E_clk_local_L, v_18_E_data_delay_H)   -- v13
BEGIN
  IF v_18_E_clk_local_L = '1' THEN
    v_18_E_data_delay_H_inv <= not (v_18_E_data_delay_H);
  END IF;
END PROCESS;
END;
```

- Resultats d'analyse avec Hytech :

```
Checking automaton Ass_q_0
Checking automaton Ass_v_18_e_net81
Checking automaton Ass_v_18_e_net85
Checking automaton Ass_v_18_e_net83
Checking automaton Ass_v_18_e_data_delay_h
Checking automaton Ass_v_17_12_10_net13
Checking automaton Ass_clk_h
Checking automaton Ass_v_18_e_clk_local_l
Checking automaton Ass_v_17_12_10_net96
Checking automaton Ass_v_17_12_10_ext_cs_h

Checking automaton P_reg10
Checking automaton B1_reg10
Checking automaton P_reg12
Checking automaton B1_reg12
Checking automaton Ass_v_17_12_clk_sig_h
Checking automaton Ass_v_17_12_10_net41
Checking automaton env

 WARNING: locn env_init of automaton env has no incoming transitions
Composing automata *********ABORTING
============================================================
Max memory used =     0 pages =         0 bytes =   0.00 MB
Time spent      =     179.98u +     13.62s =     193.60 sec total
============================================================
Program aborted. Out of memory
```

Comme on voit, l'outil hytech ne supporte pas l'analyse de cette description, contrairement à l'outil uppaal. Mais pour des raisons du temps, nous n'avons pas testé cette description. Nous analysons la version optimisée suivante qu'on peut faire passer sur l'outil hytech.

1.2. La description exp1_gf.hy

Elle est générée avec les options :

- version éclatée : non.
- optimisation des gardes simples : oui
- optimisation de la figure : oui

La description contient :

- 447 lignes.
- 8 automates (l'automate d'environnement inclus aussi).
- 8 horloges.
- 10 variables discrètes.
- 18 paramètres.

- Resultats d'analyse avec différents environnements :

L'analyse de la description hytech a été effectuée sur cinq environnements. Tous les délais des signaux des quatre premiers environnements sont égaux à 1. En revanche, les délais des signaux du dernier environnement sont donnés comme suit :

- delta0(reg12) = delta1(reg12) = 18 ,
- delta0(reg10) = delta1(reg10) = 10 ,
-
- delta0(v_17_12_10_ext_cs_h) = delta1(v_17_12_10_ext_cs_h) = 7 ,
- delta0(v_17_12_10_net96) = delta1(v_17_12_10_net96),
-
- delta0(v_18_e_clk_local_l) = delta1(v_18_e_clk_local_l) = 7 ,
- delta0(clk_h) = delta1(clk_h) = 6 ,
- delta0(v_17_12_10_net41) = delta1(v_17_12_10_net41),
- delta0(v_17_12_clk_sig_h) = delta1(v_17_12_clk_sig_h),
- delta0(v_17_12_10_net13) = delta1(v_17_12_10_net13),
- delta0(v_18_e_data_delay_h) = delta1(v_18_e_data_delay_h) = 28 ,
- delta0(v_18_e_net83) = delta1(v_18_e_net83),
- delta0(v_18_e_net85) = delta1(v_18_e_net85) = 25 ,
- delta0(v_18_e_net81) = delta1(v_18_e_net81) = 25 ,
-
- delta(q_0) = delta1(q_0) = 12;

On note aussi que la propriété de stabilité des valeurs des signaux de sortie et intermédiaires du circuit, mentionnée ci-dessous est vérifiée sur le graphe d'accessibilité dans les environnements.

- empty(atteign_reg & final_reg), tel que :
  atteign_reg := reach forward from init_reg endreach.
  final_reg := loc[P_reg12] = l_f_P_reg12 & ~ (v_18_e_clk_local_l = 1 & v_18_e_data_delay_h_inv = 1 – v_18_e_data_delay_h) | loc[P_reg10] = l_f_P_reg10 & ~ (ck = 0 & v_17_12_10_ext_cs_n = 1 - v_17_12_10_ext_cs_h) | loc[Ass_v_17_12_10_ext_cs_h] = l_f_v_17_12_10_ext_cs_h & ~ (v_17_12_10_ext_cs_h = csn) | loc[Ass_v_18_e_clk_local_l] = l_f_v_18_e_clk_local_l & ~ (v_18_e_clk_local_l = v_17_12_10_net13) | loc[Ass_v_17_12_10_net13] = l_f_v_17_12_10_net13 & ~ (v_17_12_10_net13 = 1 - ck | v_17_12_10_net13 = 1 - v_17_12_10_ext_cs_n) | loc[Ass_v_18_e_data_delay_h] = l_f_v_18_e_data_delay_h & ~ (v_18_e_data_delay_h = d_0) | loc[Ass_q_0] = l_f_q_0 & ~ (q_0 = v_18_e_data_delay_h_inv) ;

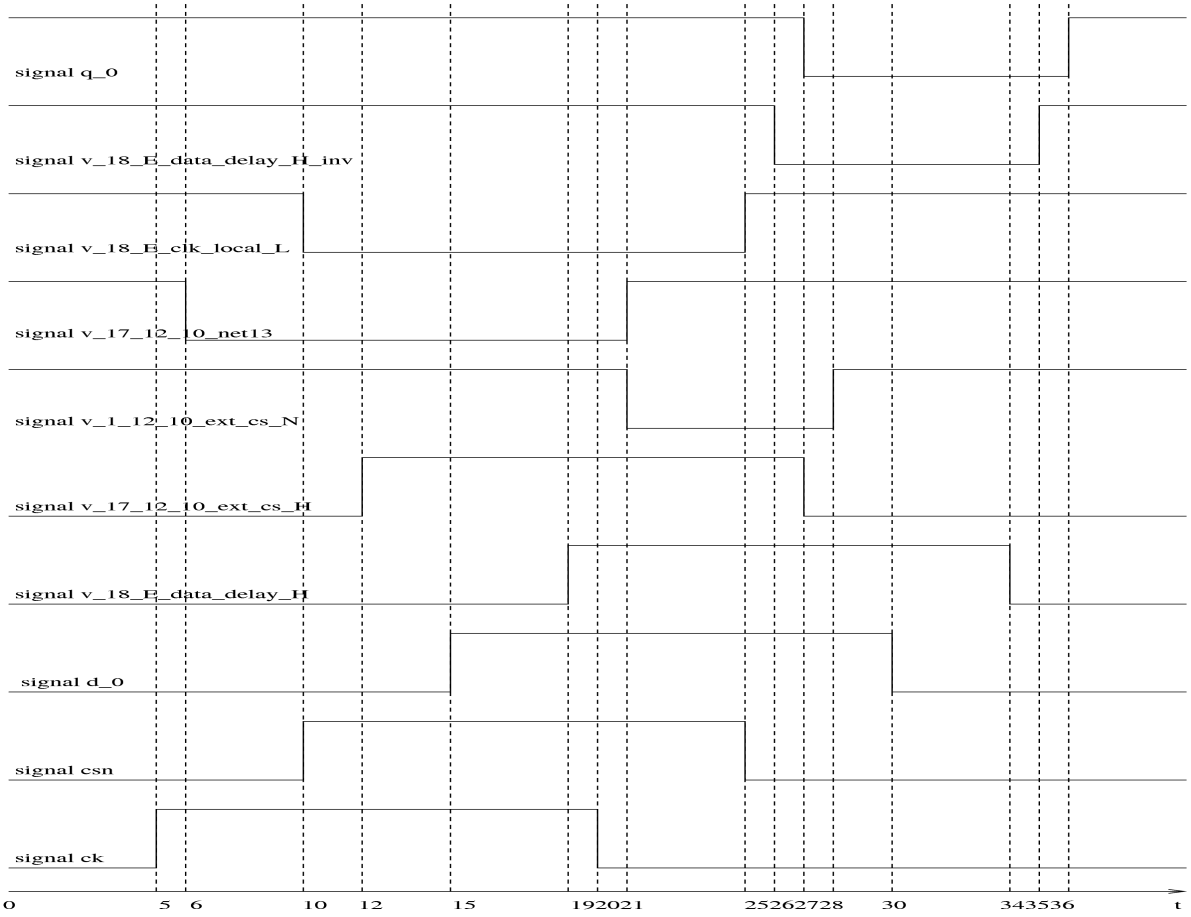
Cette dernière propriété est exprimée dans uppaal par l'ensemble des propriétés suivantes :

- A[] (P_reg12_i1.l_f_P_reg12 imply (v_18_e_clk_local_l == 1 and v_18_e_data_delay_h_inv == not

(v_18_e_data_delay_h))) .

- A[] (P_reg10_i1.l_f_P_reg10 imply (ck == 0 and v_17_12_10_ext_cs_n == not (v_17_12_10_ext_cs_h))) .
- A[] (Ass_v_17_12_10_ext_cs_h_i1.l_f_v_17_12_10_ext_cs_h imply (v_17_12_10_ext_cs_h == csn)) .
- A[] (Ass_v_18_e_clk_local_l_i1.l_f_v_18_e_clk_local_l imply (v_18_e_clk_local_l == v_17_12_10_net13)) .
- A[] (Ass_v_17_12_10_net13_i1.l_f_v_17_12_10_net13 imply (v_17_12_10_net13 == (not (ck) or not (v_17_12_10_ext_cs_n)))) .
- A[] (Ass_v_18_e_data_delay_h_i1.l_f_v_18_e_data_delay_h imply (v_18_e_data_delay_h == d_0)) .
- A[] (Ass_q_0_i1.l_f_q_0 imply (q_0 == v_18_e_data_delay_h_inv)).

Environnement env1:



- Resultats d'analyse avec Hytech :

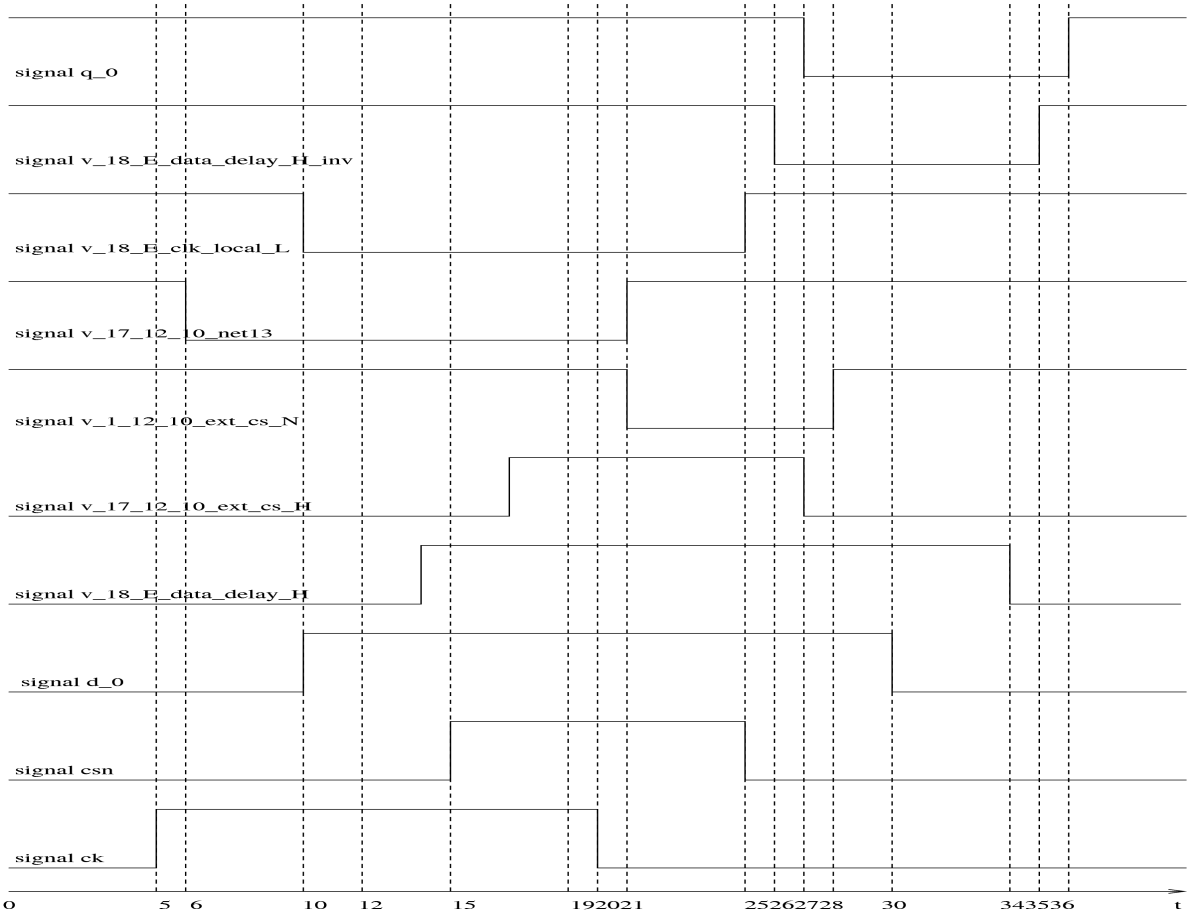
```
Checking automaton Ass_q_0
Checking automaton Ass_v_18_e_data_delay_h
Checking automaton Ass_v_17_12_10_net13
Checking automaton Ass_v_18_e_clk_local_l
Checking automaton Ass_v_17_12_10_ext_cs_h
Checking automaton P_reg10
Checking automaton P_reg12
Checking automaton env_nd_signals
  WARNING: locn env_nd_signals_0 of automaton env_nd_signals has no incoming
transitions
Composing automata *******
.....................Number of iterations required for reachability: 21

atteign:
--------
Location:
env_nd_signals_0.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
       ck  =  0     &  v_17_12_10_ext_cs_h  =  0     &  v_18_e_clk_local_l  =  1     &
v_17_12_10_net13  =  1      &  v_18_e_data_delay_h  =  0      &  q_0  =  1      &
v_17_12_10_ext_cs_n = 1    & v_18_e_data_delay_h_inv = 1    & d_0 = 0    & csn = 0
& t >= 0    & t <= 5
Location:
env_nd_signals_1.l_f_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_x0_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
```

```
       ck = 1    & v_17_12_10_ext_cs_h = 0    & v_18_e_clk_local_l = 1    &
v_17_12_10_net13  =  1      &  v_18_e_data_delay_h  =  0      &  q_0  =  1      &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& t <= 6   & t >= 5
Location:
env_nd_signals_1.l_f_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_x0_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
       ck = 1    & v_17_12_10_ext_cs_h = 0    & v_18_e_clk_local_l = 1    &
v_17_12_10_net13  =  0      &  v_18_e_data_delay_h  =  0      &  q_0  =  1      &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& t >= 6   & t <= 10

Location:
env_nd_signals_2.l_f_P_reg12.l_s_P_reg10.l_x1_v_17_12_10_ext_cs_h.l_x0_v_18_e_cl
k_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
       t = 10    & v_17_12_10_ext_cs_h = 0    & v_18_e_clk_local_l = 1    &
v_17_12_10_net13  =  0      &  v_18_e_data_delay_h  =  0      &  q_0  =  1      &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 1
& ck = 1
Location:
env_nd_signals_1.l_s_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
       t = 10    & v_17_12_10_ext_cs_h = 0    & v_18_e_clk_local_l = 0    &
v_17_12_10_net13  =  0      &  v_18_e_data_delay_h  =  0      &  q_0  =  1      &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& ck = 1

Location:
env_nd_signals_2.l_s_P_reg12.l_s_P_reg10.l_x1_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
       ck = 1    & v_17_12_10_ext_cs_h = 0    & v_18_e_clk_local_l = 0    &
v_17_12_10_net13  =  0      &  v_18_e_data_delay_h  =  0      &  q_0  =  1      &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 1
& t <= 12   & t >= 10
Location:
env_nd_signals_2.l_s_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
       ck = 1    & v_17_12_10_ext_cs_h = 1    & v_18_e_clk_local_l = 0    &
v_17_12_10_net13  =  0      &  v_18_e_data_delay_h  =  0      &  q_0  =  1      &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 1
& t >= 12   & t <= 15

Location:
env_nd_signals_3.l_s_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_x1_v_18_e_data_delay_h.l_f_q_0
       ck = 1    & v_17_12_10_ext_cs_h = 1    & v_18_e_clk_local_l = 0    &
v_17_12_10_net13  =  0      &  v_18_e_data_delay_h  =  0      &  q_0  =  1      &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& t <= 19   & t >= 15
Location:
env_nd_signals_3.l_s_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
       ck = 1    & v_17_12_10_ext_cs_h = 1    & v_18_e_clk_local_l = 0    &
v_17_12_10_net13  =  0      &  v_18_e_data_delay_h  =  1      &  q_0  =  1      &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& t >= 19   & t <= 20

Location:
env_nd_signals_4.l_s_P_reg12.l_x0_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_x1_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
       ck = 0    & v_17_12_10_ext_cs_h = 1    & v_18_e_clk_local_l = 0    &
v_17_12_10_net13  =  0      &  v_18_e_data_delay_h  =  1      &  q_0  =  1      &
```

```
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& t >= 20   & t <= 21

Location:
env_nd_signals_4.l_s_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_x1_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
       t = 21    & v_17_12_10_ext_cs_h = 1    & v_18_e_clk_local_l = 0    &
v_17_12_10_net13  =  0      &  v_18_e_data_delay_h  =  1      &  q_0  =  1      &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& ck = 0
Location:
env_nd_signals_4.l_s_P_reg12.l_x0_P_reg10.l_f_v_17_12_10_ext_cs_h.l_x1_v_18_e_cl
k_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
       t = 21    & v_17_12_10_ext_cs_h = 1    & v_18_e_clk_local_l = 0    &
v_17_12_10_net13  =  1      &  v_18_e_data_delay_h  =  1      &  q_0  =  1      &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& ck = 0

Location:
env_nd_signals_4.l_s_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_x1_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
       ck = 0    & v_17_12_10_ext_cs_h = 1    & v_18_e_clk_local_l = 0    &
v_17_12_10_net13  =  1      &  v_18_e_data_delay_h  =  1      &  q_0  =  1      &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& t >= 21   & t <= 25

Location:
env_nd_signals_4.l_x0_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
       t = 25    & v_17_12_10_ext_cs_h = 1    & v_18_e_clk_local_l = 1    &
v_17_12_10_net13  =  1      &  v_18_e_data_delay_h  =  1      &  q_0  =  1      &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& ck = 0
Location:
env_nd_signals_5.l_s_P_reg12.l_f_P_reg10.l_x0_v_17_12_10_ext_cs_h.l_x1_v_18_e_cl
k_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
       t = 25    & v_17_12_10_ext_cs_h = 1    & v_18_e_clk_local_l = 0    &
v_17_12_10_net13  =  1      &  v_18_e_data_delay_h  =  1      &  q_0  =  1      &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 0
& ck = 0

Location:
env_nd_signals_5.l_x0_P_reg12.l_f_P_reg10.l_x0_v_17_12_10_ext_cs_h.l_f_v_18_e_cl
k_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
       ck = 0    & v_17_12_10_ext_cs_h = 1    & v_18_e_clk_local_l = 1    &
v_17_12_10_net13  =  1      &  v_18_e_data_delay_h  =  1      &  q_0  =  1      &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 0
& t <= 26   & t >= 25
Location:
env_nd_signals_5.l_f_P_reg12.l_f_P_reg10.l_x0_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_x0_q_0
       ck = 0    & v_17_12_10_ext_cs_h = 1    & v_18_e_clk_local_l = 1    &
v_17_12_10_net13  =  1      &  v_18_e_data_delay_h  =  1      &  q_0  =  1      &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 1   & csn = 0
& t >= 26   & t <= 27

Location:
env_nd_signals_5.l_f_P_reg12.l_x1_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_x0_q_0
       t = 27    & v_17_12_10_ext_cs_h = 0    & v_18_e_clk_local_l = 1    &
v_17_12_10_net13  =  1      &  v_18_e_data_delay_h  =  1      &  q_0  =  1      &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 1   & csn = 0
```

```
& ck = 0
Location:
env_nd_signals_5.l_f_P_reg12.l_f_P_reg10.l_x0_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
       t = 27    & v_17_12_10_ext_cs_h = 1    & v_18_e_clk_local_l = 1    &
v_17_12_10_net13 = 1      & v_18_e_data_delay_h = 1      & q_0 = 0      &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 1   & csn = 0
& ck = 0

Location:
env_nd_signals_5.l_f_P_reg12.l_x1_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
       ck = 0    & v_17_12_10_ext_cs_h = 0    & v_18_e_clk_local_l = 1    &
v_17_12_10_net13 = 1      & v_18_e_data_delay_h = 1      & q_0 = 0      &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 1   & csn = 0
& t <= 28   & t >= 27
Location:
env_nd_signals_5.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
       ck = 0    & v_17_12_10_ext_cs_h = 0    & v_18_e_clk_local_l = 1    &
v_17_12_10_net13 = 1      & v_18_e_data_delay_h = 1      & q_0 = 0      &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 0   & d_0 = 1   & csn = 0
& t >= 28   & t <= 30

Location:
env_nd_signals_end.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_cl
k_local_l.l_f_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_f_q_0
       ck = 0    & v_17_12_10_ext_cs_h = 0    & v_18_e_clk_local_l = 1    &
v_17_12_10_net13 = 1      & v_18_e_data_delay_h = 1      & q_0 = 0      &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 0
& t >= 30   & t <= 34
Location:
env_nd_signals_end.l_x1_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_c
lk_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
       ck = 0    & v_17_12_10_ext_cs_h = 0    & v_18_e_clk_local_l = 1    &
v_17_12_10_net13 = 1      & v_18_e_data_delay_h = 0      & q_0 = 0      &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 0
& t >= 34   & t <= 35
Location:
env_nd_signals_end.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_cl
k_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_x1_q_0
       ck = 0    & v_17_12_10_ext_cs_h = 0    & v_18_e_clk_local_l = 1    &
v_17_12_10_net13 = 1      & v_18_e_data_delay_h = 0      & q_0 = 0      &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& t >= 35   & t <= 36
Location:
env_nd_signals_end.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_cl
k_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
         v_18_e_data_delay_h_inv = 1      & v_17_12_10_ext_cs_h = 0      &
v_18_e_clk_local_l = 1   & v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   &
q_0 = 1   & v_17_12_10_ext_cs_n = 1   & ck = 0   & d_0 = 0   & csn = 0   & t >=
36
```

Environnement env2:



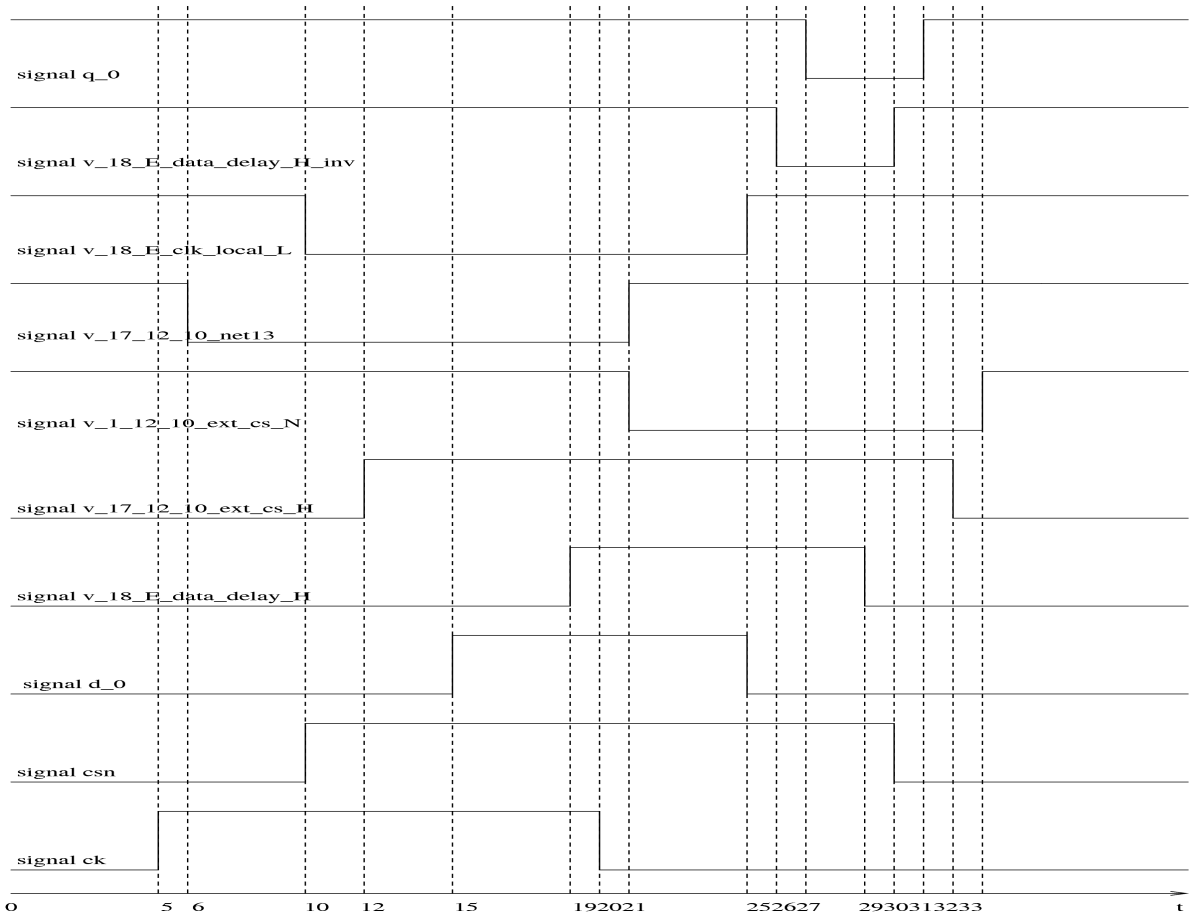

```
Checking automaton Ass_q_0
Checking automaton Ass_v_18_e_data_delay_h
Checking automaton Ass_v_17_12_10_net13
Checking automaton Ass_v_18_e_clk_local_l
Checking automaton Ass_v_17_12_10_ext_cs_h
Checking automaton P_reg10
Checking automaton P_reg12
Checking automaton env_nd_signals
 WARNING: locn env_nd_signals_0 of automaton env_nd_signals has no incoming
transitions
Composing automata *******
.....................Number of iterations required for reachability: 21

atteign:
--------
Location:
env_nd_signals_0.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& t >= 0   & t <= 5
Location:
env_nd_signals_1.l_f_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_x0_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
```

```
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& t <= 6   & t >= 5
Location:
env_nd_signals_1.l_f_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_x0_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& t >= 6   & t <= 10

Location:
env_nd_signals_2.l_f_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_x0_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_x1_v_18_e_data_delay_h.l_f_q_0
     t = 10   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 0
& ck = 1
Location:
env_nd_signals_1.l_s_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     t = 10   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& ck = 1

Location:
env_nd_signals_2.l_s_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_x1_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 0
& t <= 14   & t >= 10
Location:
env_nd_signals_2.l_s_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 0
& t >= 14   & t <= 15
Location:
env_nd_signals_3.l_s_P_reg12.l_s_P_reg10.l_x1_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& t <= 17   & t >= 15
Location:
env_nd_signals_3.l_s_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& t >= 17   & t <= 20

Location:
env_nd_signals_4.l_s_P_reg12.l_x0_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_x1_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& t >= 20   & t <= 21
```

```
Location:
env_nd_signals_4.l_s_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_x1_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     t = 21   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& ck = 0
Location:
env_nd_signals_4.l_s_P_reg12.l_x0_P_reg10.l_f_v_17_12_10_ext_cs_h.l_x1_v_18_e_cl
k_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     t = 21   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& ck = 0

Location:
env_nd_signals_4.l_s_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_x1_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& t >= 21   & t <= 25

Location:
env_nd_signals_4.l_x0_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     t = 25   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& ck = 0
Location:
env_nd_signals_5.l_s_P_reg12.l_f_P_reg10.l_x0_v_17_12_10_ext_cs_h.l_x1_v_18_e_cl
k_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     t = 25   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 0
& ck = 0

Location:
env_nd_signals_5.l_x0_P_reg12.l_f_P_reg10.l_x0_v_17_12_10_ext_cs_h.l_f_v_18_e_cl
k_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 0
& t <= 26   & t >= 25
Location:
env_nd_signals_5.l_f_P_reg12.l_f_P_reg10.l_x0_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_x0_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 1   & csn = 0
& t >= 26   & t <= 27

Location:
env_nd_signals_5.l_f_P_reg12.l_x1_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_x0_q_0
     t = 27   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 1   & csn = 0
& ck = 0
Location:
env_nd_signals_5.l_f_P_reg12.l_f_P_reg10.l_x0_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
```

```
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     t = 27   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 0   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 1   & csn = 0
& ck = 0

Location:
env_nd_signals_5.l_f_P_reg12.l_x1_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 0   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 1   & csn = 0
& t <= 28   & t >= 27

Location:
env_nd_signals_5.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 0   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 0   & d_0 = 1   & csn = 0
& t >= 28   & t <= 30

Location:
env_nd_signals_end.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_cl
k_local_l.l_f_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 0   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 0
& t >= 30   & t <= 34
Location:
env_nd_signals_end.l_x1_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_c
lk_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 0   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 0
& t >= 34   & t <= 35
Location:
env_nd_signals_end.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_cl
k_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_x1_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 0   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& t >= 35   & t <= 36
Location:
env_nd_signals_end.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_cl
k_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     v_18_e_data_delay_h_inv = 1   & v_17_12_10_ext_cs_h = 0   &
v_18_e_clk_local_l = 1   & v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   &
q_0 = 1   & v_17_12_10_ext_cs_n = 1   & ck = 0   & d_0 = 0   & csn = 0   & t >=
36
```

Environnement env3:



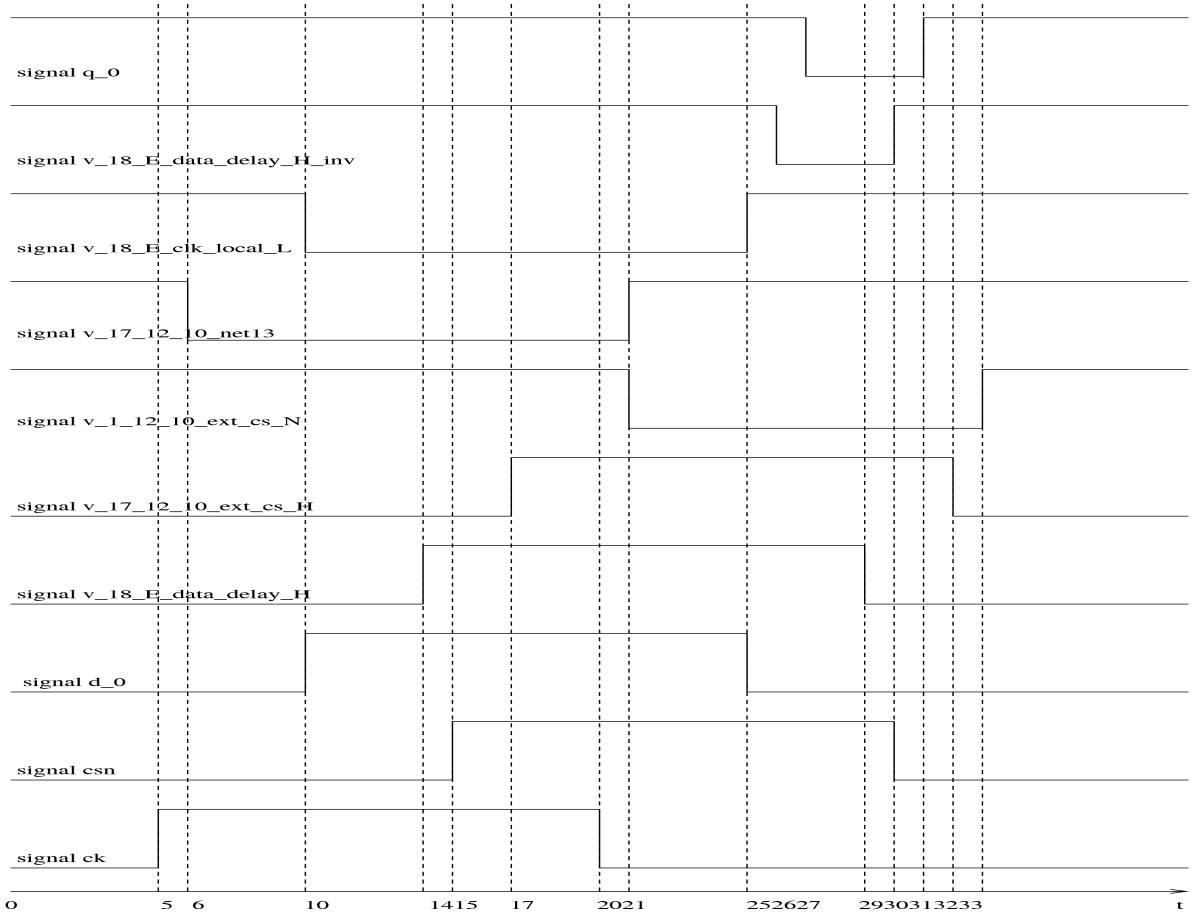

```
Checking automaton Ass_q_0
Checking automaton Ass_v_18_e_data_delay_h
Checking automaton Ass_v_17_12_10_net13
Checking automaton Ass_v_18_e_clk_local_l
Checking automaton Ass_v_17_12_10_ext_cs_h
Checking automaton P_reg10
Checking automaton P_reg12
Checking automaton env
 WARNING: locn env_nd_signals_0 of automaton env has no incoming transitions
Composing automata *******
.....................Number of iterations required for reachability: 21

atteign:
--------
Location:
env_init.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.
l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& t >= 0   & t <= 5
Location:
env_1.l_f_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_x
0_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
```

```
& t <= 6   & t >= 5
Location:
env_1.l_f_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_x0_v_18_e_clk_local_l.l_
f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& t >= 6   & t <= 10

Location:
env_2.l_f_P_reg12.l_s_P_reg10.l_x1_v_17_12_10_ext_cs_h.l_x0_v_18_e_clk_local_l.l
_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     t = 10   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 1
& ck = 1
Location:
env_1.l_s_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_f
_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     t = 10   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& ck = 1

Location:
env_2.l_s_P_reg12.l_s_P_reg10.l_x1_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_
f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 1
& t <= 12   & t >= 10
Location:
env_2.l_s_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_f
_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 1
& t >= 12   & t <= 15
Location:
env_3.l_s_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_f
_v_17_12_10_net13.l_x1_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& t <= 19   & t >= 15
Location:
env_3.l_s_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_f
_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& t >= 19   & t <= 20

Location:
env_4.l_s_P_reg12.l_x0_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_
x1_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& t >= 20   & t <= 21

Location:
```

```
env_4.l_s_P_reg12.l_x0_P_reg10.l_f_v_17_12_10_ext_cs_h.l_x1_v_18_e_clk_local_l.l
_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     t = 21   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& ck = 0
Location:
env_4.l_s_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_x
1_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     t = 21   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& ck = 0

Location:
env_4.l_s_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_x1_v_18_e_clk_local_l.l_
f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& t >= 21   & t <= 25

Location:
env_5.l_s_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_x1_v_18_e_clk_local_l.l_
f_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_f_q_0
     t = 25   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 1
& ck = 0
Location:
env_4.l_x0_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_
f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     t = 25   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& ck = 0

Location:
env_5.l_x0_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_
f_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 1
& t <= 26   & t >= 25
Location:
env_5.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_f
_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_x0_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 1
& t <= 27   & t >= 26
Location:
env_5.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_f
_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 0   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 1
& t <= 29   & t >= 27
Location:
env_5.l_x1_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_
f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
```

```
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 0   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 1
& t >= 29   & t <= 30

Location:
env_5.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_f
_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_x1_q_0
     t = 30   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 0   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 1
& ck = 0
Location:
env_end.l_x1_P_reg12.l_f_P_reg10.l_x0_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l
.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     t = 30   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 0   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 0
& ck = 0

Location:
env_end.l_f_P_reg12.l_f_P_reg10.l_x0_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.
l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_x1_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 0   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& t <= 31   & t >= 30
Location:
env_end.l_f_P_reg12.l_f_P_reg10.l_x0_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.
l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& t >= 31   & t <= 32
Location:
env_end.l_f_P_reg12.l_x1_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.
l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& t >= 32   & t <= 33
Location:
env_end.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l
_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     v_18_e_data_delay_h_inv = 1   & v_17_12_10_ext_cs_h = 0   &
v_18_e_clk_local_l = 1   & v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   &
q_0 = 1   & v_17_12_10_ext_cs_n = 1   & ck = 0   & d_0 = 0   & csn = 0   & t >=
33
```

Environnement env4:




```
Checking automaton Ass_q_0
Checking automaton Ass_v_18_e_data_delay_h
Checking automaton Ass_v_17_12_10_net13
Checking automaton Ass_v_18_e_clk_local_l
Checking automaton Ass_v_17_12_10_ext_cs_h
Checking automaton P_reg10
Checking automaton P_reg12
Checking automaton env
 WARNING: locn env_nd_signals_0 of automaton env has no incoming transitions
Composing automata *******
.....................Number of iterations required for reachability: 21

atteign:
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Location:
env_init.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.
l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& t >= 0   & t <= 5
Location:
env_1.l_f_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_x
0_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
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& t <= 6   & t >= 5
Location:
env_1.l_f_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_x0_v_18_e_clk_local_l.l_
f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& t >= 6   & t <= 10

Location:
env_1.l_s_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_f
_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     t = 10   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& ck = 1
Location:
env_2.l_f_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_x0_v_18_e_clk_local_l.l_
f_v_17_12_10_net13.l_x1_v_18_e_data_delay_h.l_f_q_0
     t = 10   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 0
& ck = 1

Location:
env_2.l_s_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_f
_v_17_12_10_net13.l_x1_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 0
& t <= 14   & t >= 10
Location:
env_2.l_s_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_f
_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 0
& t >= 14   & t <= 15
Location:
env_3.l_s_P_reg12.l_s_P_reg10.l_x1_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_
f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& t <= 17   & t >= 15
Location:
env_3.l_s_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_f
_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& t >= 17   & t <= 20

Location:
env_4.l_s_P_reg12.l_x0_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_
x1_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& t >= 20   & t <= 21

Location:
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env_4.l_s_P_reg12.l_x0_P_reg10.l_f_v_17_12_10_ext_cs_h.l_x1_v_18_e_clk_local_l.l
_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     t = 21   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& ck = 0
Location:
env_4.l_s_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_x
1_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     t = 21   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& ck = 0

Location:
env_4.l_s_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_x1_v_18_e_clk_local_l.l_
f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& t >= 21   & t <= 25

Location:
env_4.l_x0_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_
f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     t = 25   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& ck = 0
Location:
env_5.l_s_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_x1_v_18_e_clk_local_l.l_
f_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_f_q_0
     t = 25   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 1
& ck = 0

Location:
env_5.l_x0_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_
f_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 1
& t <= 26   & t >= 25
Location:
env_5.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_f
_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_x0_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 1
& t <= 27   & t >= 26
Location:
env_5.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_f
_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 0   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 1
& t <= 29   & t >= 27
Location:
env_5.l_x1_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_
f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
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v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 0   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 1
& t >= 29   & t <= 30

Location:
env_5.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l_f
_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_x1_q_0
     t = 30   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 0   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 1
& ck = 0
Location:
env_end.l_x1_P_reg12.l_f_P_reg10.l_x0_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l
.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     t = 30   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 0   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 0
& ck = 0

Location:
env_end.l_f_P_reg12.l_f_P_reg10.l_x0_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.
l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_x1_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 0   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& t <= 31   & t >= 30
Location:
env_end.l_f_P_reg12.l_f_P_reg10.l_x0_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.
l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& t >= 31   & t <= 32
Location:
env_end.l_f_P_reg12.l_x1_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.
l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& t >= 32   & t <= 33
Location:
env_end.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_local_l.l
_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     v_18_e_data_delay_h_inv = 1   & v_17_12_10_ext_cs_h = 0   &
v_18_e_clk_local_l = 1   & v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   &
q_0 = 1   & v_17_12_10_ext_cs_n = 1   & ck = 0   & d_0 = 0   & csn = 0   & t >=
33
```
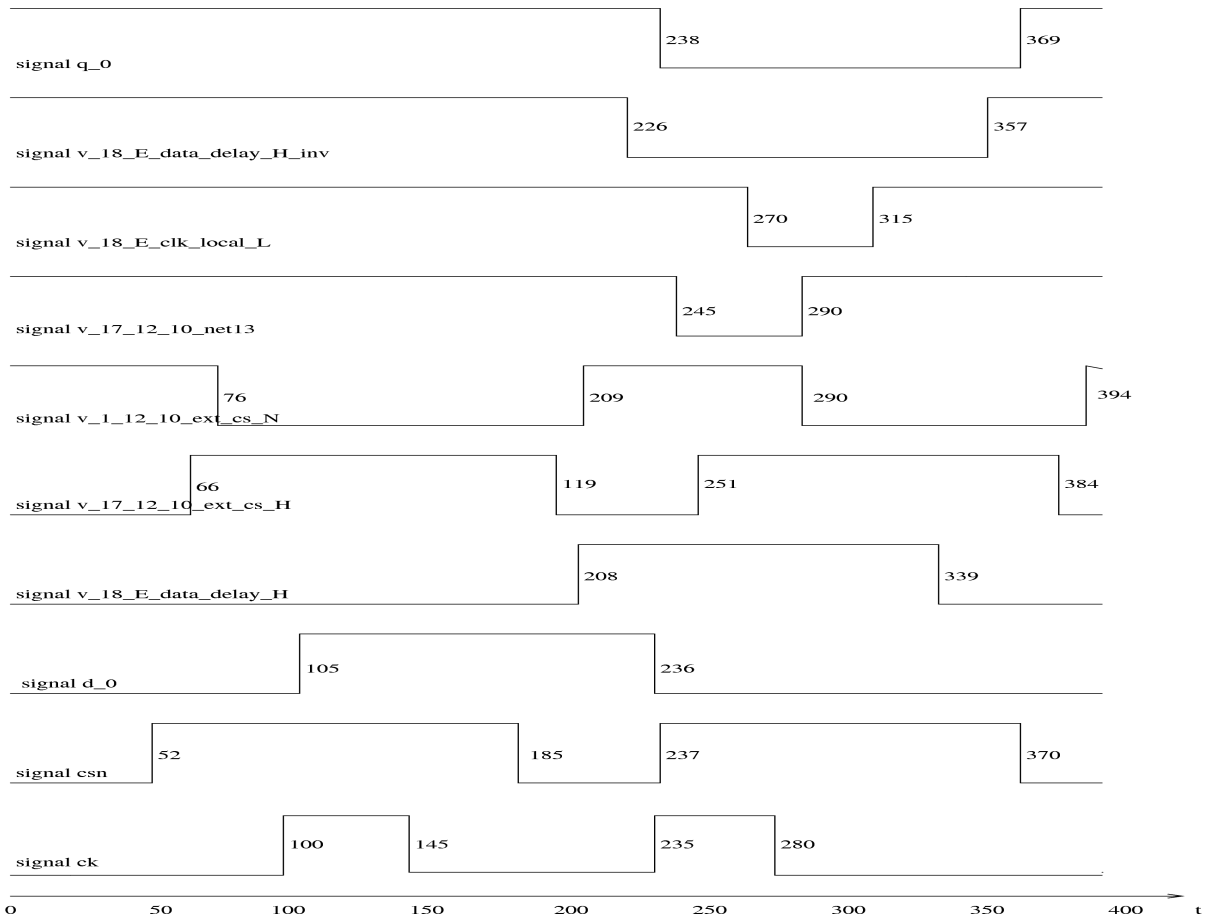

Environnement 5:




```
Checking automaton Ass_q_0
Checking automaton Ass_v_18_e_data_delay_h
Checking automaton Ass_v_17_12_10_net13
Checking automaton Ass_v_18_e_clk_local_l
Checking automaton Ass_v_17_12_10_ext_cs_h
Checking automaton P_reg10
Checking automaton P_reg12
Checking automaton env_nd_signals
 WARNING: locn env_nd_signals_0 of automaton env_nd_signals has no incoming
transitions
Composing automata *******
.............................Number of iterations required for reachability: 29

atteign:
--------
Location:
env_nd_signals_0.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& t >= 0   & t <= 52
Location:
env_nd_signals_1.l_f_P_reg12.l_f_P_reg10.l_x1_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
```

```
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 1
& t <= 66   & t >= 52
Location:
env_nd_signals_1.l_f_P_reg12.l_x0_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 1
& t <= 76   & t >= 66
Location:
env_nd_signals_1.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 1
& t >= 76   & t <= 100
Location:
env_nd_signals_2.l_f_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 1
& t >= 100   & t <= 105
Location:
env_nd_signals_3.l_f_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_x1_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& t >= 105   & t <= 145
Location:
env_nd_signals_4.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_x1_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 1
& t >= 145   & t <= 185
Location:
env_nd_signals_5.l_f_P_reg12.l_f_P_reg10.l_x0_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_x1_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 0
& t <= 199   & t >= 185

Location:
env_nd_signals_5.l_f_P_reg12.l_x1_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_x1_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 0
& t <= 208   & t >= 199
Location:
env_nd_signals_5.l_x0_P_reg12.l_x1_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_cl
k_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 0
& t <= 209   & t >= 208
Location:
env_nd_signals_5.l_x0_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
```

```
     ck = 0   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 1   & d_0 = 1   & csn = 0
& t <= 226   & t >= 209
Location:
env_nd_signals_5.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_x0_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 0   & d_0 = 1   & csn = 0
& t >= 226   & t <= 235
Location:
env_nd_signals_6.l_f_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_x0_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_x0_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 0   & d_0 = 1   & csn = 0
& t >= 235   & t <= 236
Location:
env_nd_signals_7.l_f_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_x0_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_x0_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 0
& t >= 236   & t <= 237
Location:
env_nd_signals_8.l_f_P_reg12.l_s_P_reg10.l_x1_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_x0_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_x0_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 1   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 1
& t <= 238   & t >= 237
Location:
env_nd_signals_8.l_f_P_reg12.l_s_P_reg10.l_x1_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_x0_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 0   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 1
& t <= 245   & t >= 238
Location:
env_nd_signals_8.l_f_P_reg12.l_s_P_reg10.l_x1_v_17_12_10_ext_cs_h.l_x0_v_18_e_cl
k_local_l.l_f_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 1   & q_0 = 0   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 1
& t <= 251   & t >= 245
Location:
env_nd_signals_8.l_f_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_x0_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 1   & q_0 = 0   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 1
& t <= 270   & t >= 251
Location:
env_nd_signals_8.l_s_P_reg12.l_s_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_f_q_0
     ck = 1   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 1   & q_0 = 0   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 1
& t >= 270   & t <= 280
Location:
env_nd_signals_9.l_s_P_reg12.l_x0_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
```

```
_local_l.l_x1_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 1   & q_0 = 0   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 1
& t >= 280   & t <= 290

Location:
env_nd_signals_9.l_s_P_reg12.l_x0_P_reg10.l_f_v_17_12_10_ext_cs_h.l_x1_v_18_e_cl
k_local_l.l_f_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_f_q_0
     t = 290   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 0   &
v_17_12_10_ext_cs_n = 1   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 1
& ck = 0
Location:
env_nd_signals_9.l_s_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_x1_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_f_q_0
     t = 290   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 0   & v_18_e_data_delay_h = 1   & q_0 = 0   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 1
& ck = 0

Location:
env_nd_signals_9.l_s_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_x1_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 0   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 0   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 1
& t <= 310   & t >= 290
Location:
env_nd_signals_9.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_x0_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 1   & q_0 = 0   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 1
& t <= 339   & t >= 310
Location:
env_nd_signals_9.l_x1_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk
_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 0   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 0   & d_0 = 0   & csn = 1
& t <= 357   & t >= 339
Location:
env_nd_signals_9.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_x1_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 0   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 1
& t <= 369   & t >= 357
Location:
env_nd_signals_9.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_clk_
local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 1
& t >= 369   & t <= 370
Location:
env_nd_signals_end.l_f_P_reg12.l_f_P_reg10.l_x0_v_17_12_10_ext_cs_h.l_f_v_18_e_c
lk_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 1   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
```

```
& t >= 370   & t <= 384
Location:
env_nd_signals_end.l_f_P_reg12.l_x1_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_c
lk_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     ck = 0   & v_17_12_10_ext_cs_h = 0   & v_18_e_clk_local_l = 1   &
v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   & q_0 = 1   &
v_17_12_10_ext_cs_n = 0   & v_18_e_data_delay_h_inv = 1   & d_0 = 0   & csn = 0
& t >= 384   & t <= 394
Location:
env_nd_signals_end.l_f_P_reg12.l_f_P_reg10.l_f_v_17_12_10_ext_cs_h.l_f_v_18_e_cl
k_local_l.l_f_v_17_12_10_net13.l_f_v_18_e_data_delay_h.l_f_q_0
     v_18_e_data_delay_h_inv = 1   & v_17_12_10_ext_cs_h = 0   &
v_18_e_clk_local_l = 1   & v_17_12_10_net13 = 1   & v_18_e_data_delay_h = 0   &
q_0 = 1   & v_17_12_10_ext_cs_n = 1   & ck = 0   & d_0 = 0   & csn = 0   & t >=
394
```

2. La description LSV :

Le but de cette partie est de comparer les résultats de tests obtenus sur les descriptions générées par le programme par rapport à celles qui sont décrites dans [CEFX.06a & CEFX.06c]. Tout d'abord, on rappelle ci-dessous la représentation structurelle de la description en VHDL LSV1, sous forme d'un graphe fonctionnel et temporel abstrait, associée à une implémentation de l'architecture SPSMALL.

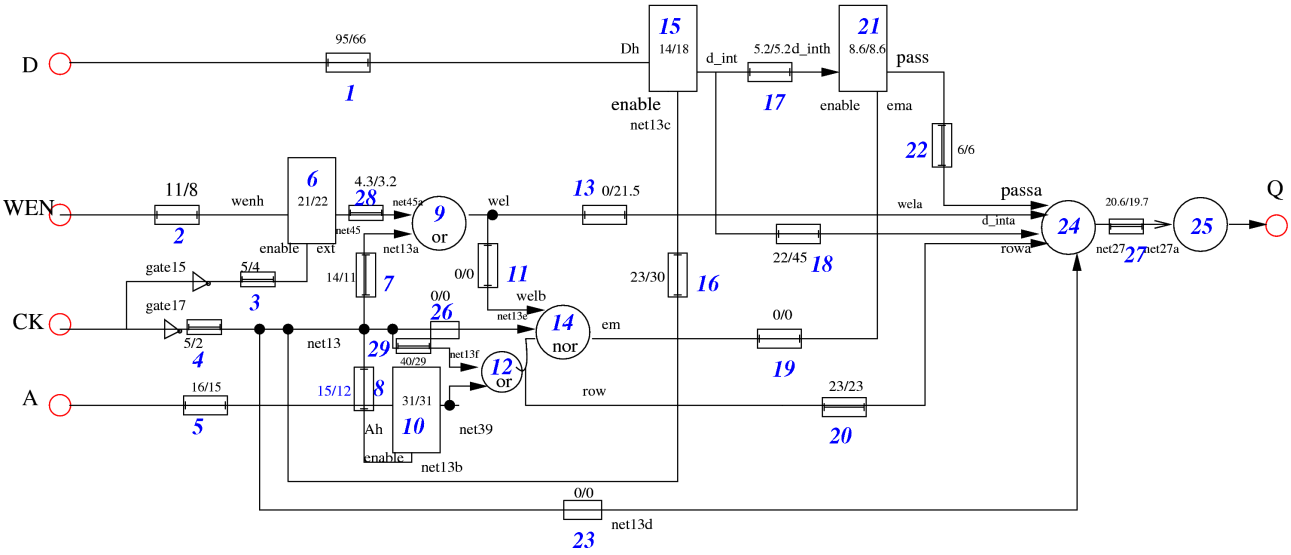


Figure 1: AFTG de SPSMALL (SP1) ([CEFX 06a]).

Ici, comme a été déjà fait dans [CEFX.06a & CEFX.06c], on va faire l'analyse des deux implémentations SP1 et SP2 de l'architecture SPSMALL. On note que ces deux dernières sont identiques au niveau de leur représentation structurelle (leur fonction est identique). En revanche, les délais de propagation de leurs composants peuvent être différents. Ils sont représentés par des graphes fonctionnels et temporels abstraits (AFTG). Comme conséquence, les descriptions en uppaal ou hytech associées à ces deux implémentations sont presque les mêmes. Elles ne diffèrent que dans les valeurs à affecter aux paramètres associés aux délais des signaux internes. La figure mentionnée ci-dessus représente l'implémentation SP1.

Le Programme en VHDL (lsv.vhd) associé au circuit mentionée ci-dessus est décrit comme suit :

```
-- description SPSMALL selon BLUEBERRIES
-- modifications pour incorporer les délais dans les portes
--    - net13 supprime : gate 17 repliquee et delai de fils sur sortie
incorpores
--    - wel supprime : gate 9 repliquee et delai de fil de sortie incorpores
--    - delai 19 (fil de sortie) incorpore dans gate 14
--    - delai 20 incorpore dans gate 12
--    - delai 3 incorpore dans gate 15

ENTITY SPSMALL_BLUEBERRIES IS
  PORT (
         Q_0 : out   BIT;
          CK : in    BIT;
         WEN : in    BIT;
         A_0 : in    BIT;
         D_0 : in    BIT
  );
END SPSMALL_BLUEBERRIES;

-- Architecture Declaration

ARCHITECTURE RTL OF SPSMALL_BLUEBERRIES IS
```

```
  SIGNAL D_h : BIT;                -- entree data latchD
  SIGNAL WEN_h : BIT;              -- entree data latchWEN
  SIGNAL A_h : BIT;                -- entree data latchA
-- SIGNAL net13 : BIT;             -- le fameux signal net13
  SIGNAL en_latchWEN : bit;        -- enable de latchWEN, nommé enable_ext
  SIGNAL en_latchA : bit;          -- enable de latchA, aussi nommé net13b
  SIGNAL en_latchD : bit;          -- enable de latchD, aussi nommé net13c
  SIGNAL D_int : bit;              -- sortie latchD
  SIGNAL net45 : bit;              -- sortie latchWEN
  SIGNAL net39 : bit;              -- sortie latchA
  SIGNAL net13a : bit;             -- retard net13
  SIGNAL net13d : bit;             -- retard net13
  SIGNAL net13e : bit;             -- retard net13
  SIGNAL net13f : bit;             -- retard net13
  SIGNAL net45a : bit;             -- retard net45
--  SIGNAL wel : bit;              -- sortie gate 9
  SIGNAL wela : bit;               -- retard wel
  SIGNAL welb : bit;               -- retard wel
  SIGNAL row : bit;                -- sortie gate 12
--  SIGNAL em : bit;               -- sortie gate 14
  SIGNAL ema : bit;                -- sortie gate 14
  SIGNAL D_inta : bit;             -- retard D_int
  SIGNAL D_int_h : bit;            -- retard D_int
  SIGNAL rowa : bit;               -- retard row
  SIGNAL pass : bit;               -- sortie point memoire
  SIGNAL passa : bit;              -- retard pass
  SIGNAL net27 : bit;              -- retard pass
BEGIN

  D_h <= D_0;                      -- chaine d'inverseurs : delai 1
  A_h <= A_0;                      -- chaine d'inverseurs : delai 5
  WEN_h <= WEN;                    -- chaine d'inverseurs : delai 2

  -- net13 <= not CK;              -- gate 17 / delai 4
  en_latchWEN <= not CK;           -- gate 15 / delai 3
  en_latchA <= not CK;             -- delai 4 (not 17) +  delai 8 (retard)
  en_latchD <= not CK;             -- delai 4 (not 17) +  delai 16 (retard)

  net13a <= not CK;                -- delai 4 (not 17) +  delai 7 (retard)
  net13d <= not CK;                -- delai 4 (not 17) +  delai 23 (retard)
  net13e <= not CK;                -- delai 4 (not 17) +  delai 26
  net13f <= not CK;                -- delai 4 (not 17) +  delai 29

  net45a <= net45;                 -- retard / net45a / delai 28

  -- wel <= net45a or net13a;      -- gate 9 / PAS DE DELAI
  wela <= net45a or net13a;        -- delai nul (or 9) + delai 13
  welb <= net45a or net13a;        -- delai nul (or 9) + delai 11

   row <= net13f or net39;         -- gate 12 / PAS DE DELAI

  -- em <= not (welb or net13e or row); -- gate 14 / PAS DE DELAI

  D_inta <= D_int;                 -- retard / D_inta / delai 18
  rowa <= net13f or net39;         -- delai nul (or 12) +  delai 20
  ema <= not ((welb or net13e) or row);  -- delai nul (nor 14) +  delai 19
  passa <= pass;              -- retard / passa / delai 22
  D_int_h <= D_int;                -- retard / D_int_h / delai 17

  Q_0 <= net27;                    -- retard / net27a / delai 27

-- les process
```

```
  REG_latchD: PROCESS (en_latchD, D_h)   -- latchD / delai 15
      begin
      if en_latchD = '1' then
         D_int <= D_h;
      end if;
      end process;

  REG_latchWEN: PROCESS (en_latchWEN,WEN_h)-- latchWEN / delai 6
      begin
      if en_latchWEN = '1' then
         net45 <= WEN_h;
      end if;
      end process;

  REG_latch_A: PROCESS (en_latchA,A_h)   -- latchA / delai 10
      begin
      if en_latchA = '1' then
         net39 <= A_h;
      end if;
      end process;

  REG_mem_point: PROCESS (ema, D_int_h) -- point memoire / delai 21
      begin
      if ema = '1' then
        pass <= D_int_h;
      end if;
      end process;

  REG_mux_output: PROCESS (passa, D_inta, wela, rowa, net13d)
      begin                    -- mux et buffer de sortie / PAS DE DELAI
      if net13d = '0' and wela = '0' then
         net27 <= D_inta;
      elsif ((net13d = '0' and wela = '1') and rowa = '1') then
         net27 <= passa;
      end if;
      end process;
END;
```

Les descriptions en hytech ou en uppaal, associées à ces implémentations SP1 et SP2, générées par la programme contiennent :

- 1553 lignes dans la description en hytech et 1291 lignes dans la description en uppaal.
- 27 automates + l'automate d'environnement.
- 28 horloges.
- 29 + 1 (i_B) + 2 (B_i) = 32 variables discrètes.
- 62 paramètres.

Resultats d'analyse avec Hytech :

```
Checking automaton Ass_q_0
Checking automaton Ass_d_h
Checking automaton Ass_wen_h
Checking automaton Ass_a_h
Checking automaton Ass_en_latchwen
Checking automaton Ass_en_latcha
Checking automaton Ass_en_latchd
Checking automaton P_reg_latchd
Checking automaton P_reg_latchwen
Checking automaton P_reg_latch_a
```

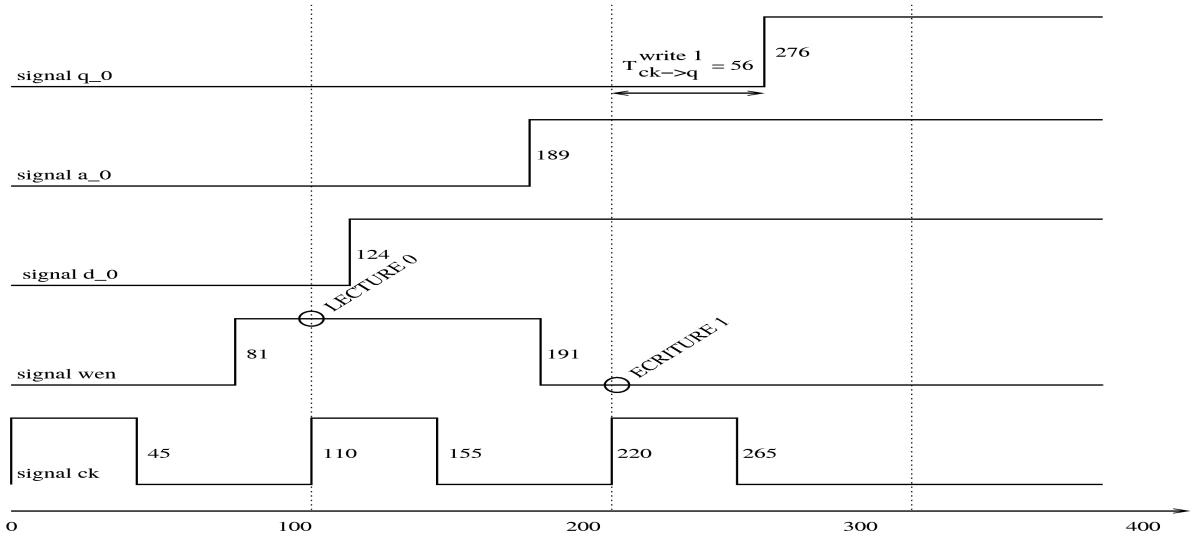
```
Checking automaton Ass_net13a
Checking automaton Ass_net13d
Checking automaton Ass_net13e
Checking automaton Ass_net13f
Checking automaton Ass_net45a
Checking automaton Ass_wela
Checking automaton Ass_welb
Checking automaton Ass_row
Checking automaton Ass_ema
Checking automaton Ass_d_inta

Checking automaton Ass_d_int_h
Checking automaton Ass_rowa
Checking automaton P_reg_mem_point
Checking automaton Ass_passa
Checking automaton P_reg_mux_output
Checking automaton B2_reg_mux_output
Checking automaton B1_reg_mux_output
Checking automaton env

 WARNING: locn env_init of automaton env has no incoming transitions
Composing automata *******ABORTING
============================================================
Max memory used =     0 pages =        0 bytes =   0.00 MB
Time spent      =     179.99u +      7.46s =     187.45 sec total
============================================================
Program aborted. Out of memory
```

Evidemment, les descriptions en hytech générées qui contiennent beaucoup d'automates ne passent pas sur l'outil Hytech. En revanche, l'outil Uppaal supporte l'analyse des descriptions de cette taille (Ceci est dû au fait déterminisme des automates). En effet, on les avait testé avec l'outil uppaal jusqu'à présent sur trois environnements différents avec lesquels on peut générer des écritures des valeurs 0 et 1 sur la sortie de l'architecture q_0.

Les résultats d'analyse sur ces trois environnements de ces classes sont décrits brièvement sur les chronogrammes suivants. Comme on voit la dessous, on a représenté que les signaux d'entrée ck, wen, d_0, a_0 et le signal de sortie q_0, pour des raisons de lisibilité.

Environnement 1:

- Avec les délais de SP1:



On note que le graphe d'atteignabilité, soit GA, associée à l'automate obtenu par la composition du modèle associé au programme vhdl et l'automate d'environnement satisfait la propriété suivante :

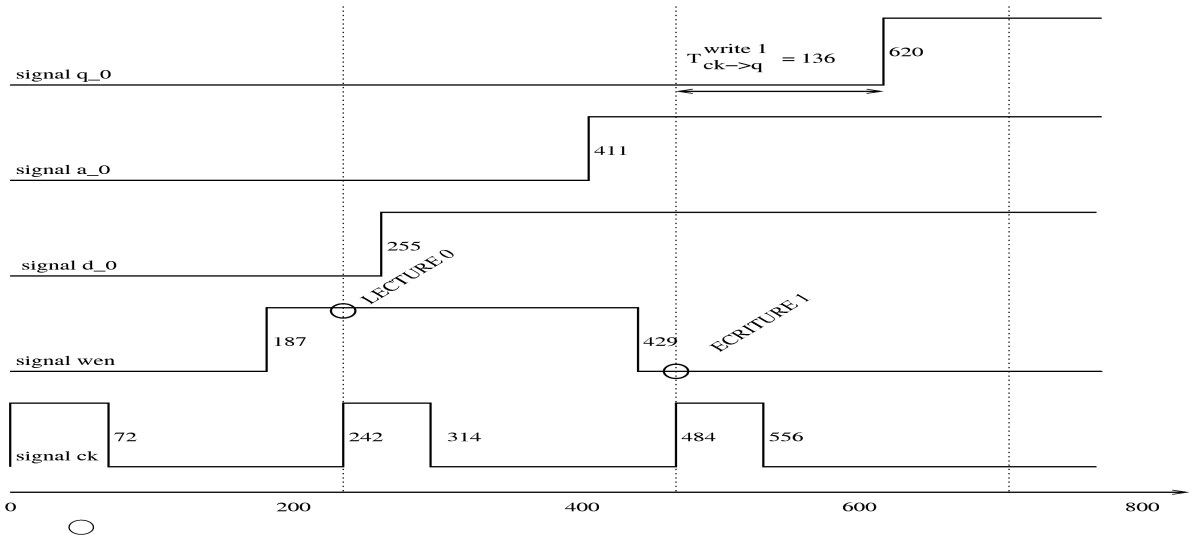
GA |= A[] ((t>156 and t<276) imply q_0 == 0) and (t>276 imply q_0 == 1))

Bien qu'il ne satisfait pas la propriété suivante :

A[] ((t>156 and t<277) imply q_0 == 0) and (t>277 imply q_0 == 1))

Donc, ça correspond bien à ce qui est décrit sur le diagramme.

- Avec les délais de SP2:

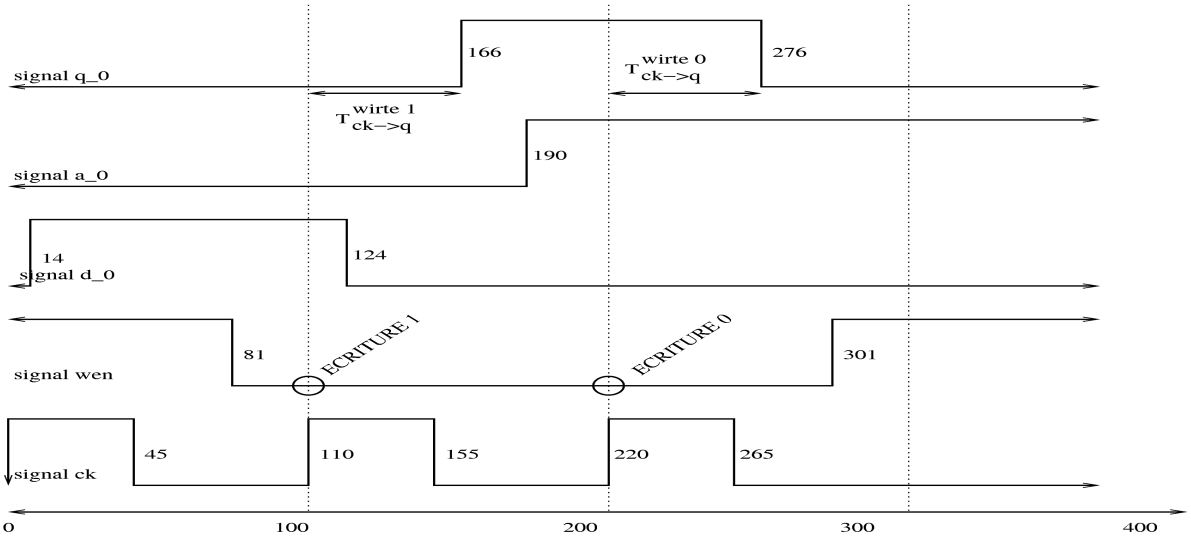


Ici, le graphe d'atteignabilité GA vérifie que :

GA |= A[] ((t>383 and t<620) imply q_0 == 0) and (t>620 imply q_0 == 1))
GA |/= A[] ((t>383 and t<621) imply q_0 == 0) and (t>621 imply q_0 == 1))

Environnement 2:

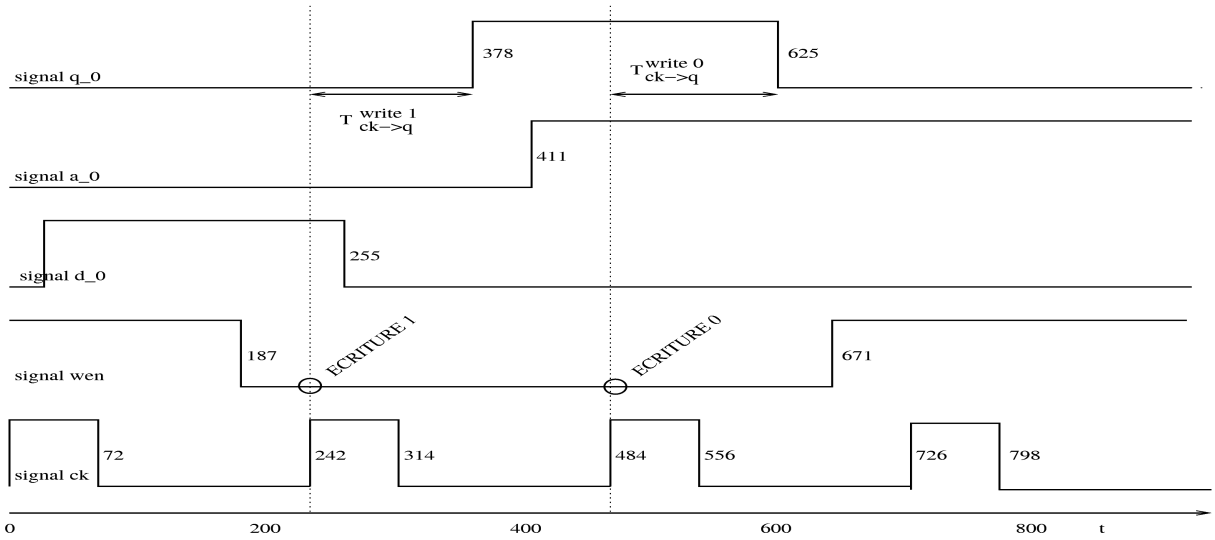
- Avec les délais de SP1:



avec le graphe d'atteignabilité obtenu GA, on a :

GA |= A[] (((t > 275) imply q_0 == 0) and ((t > 166 and t < 275) imply q_0 == 1))
GA |/= A[] (((t > 276) imply q_0 == 0) and ((t > 166 and t < 276) imply q_0 == 1))

- Avec les délais de SP2:

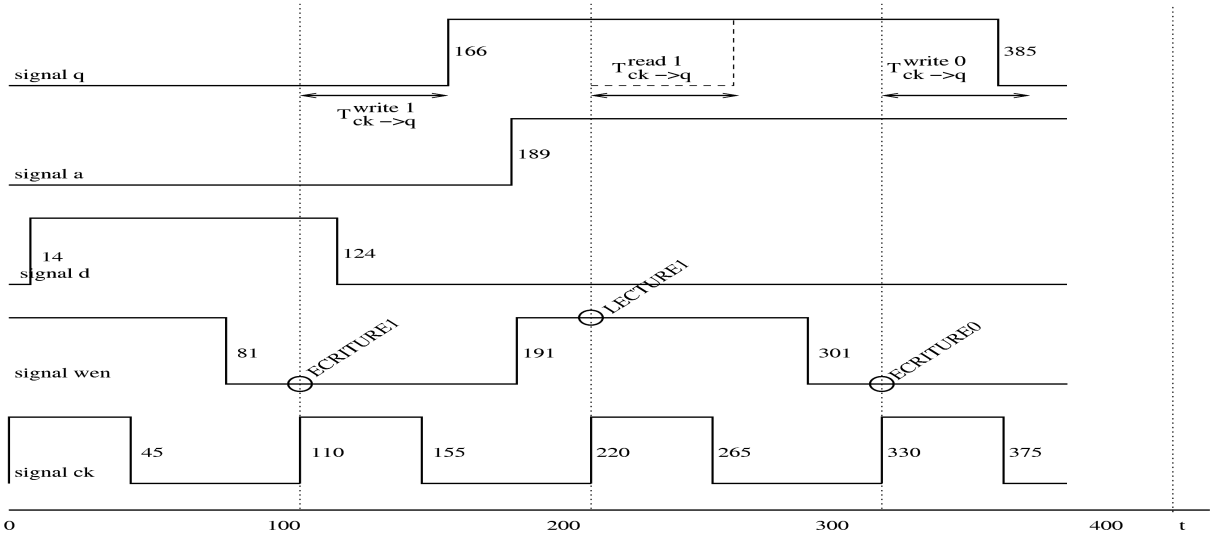


Le graphe d'atteignabilité obtenu GA vérifie ces propriétés :

GA |= A[] (((t > 625) imply q_0 == 0) and ((t > 378 and t < 625) imply q_0 == 1))
GA |/= A[] (((t > 626) imply q_0 == 0) and ((t > 378 and t < 626) imply q_0 == 1))

Environnement 3:

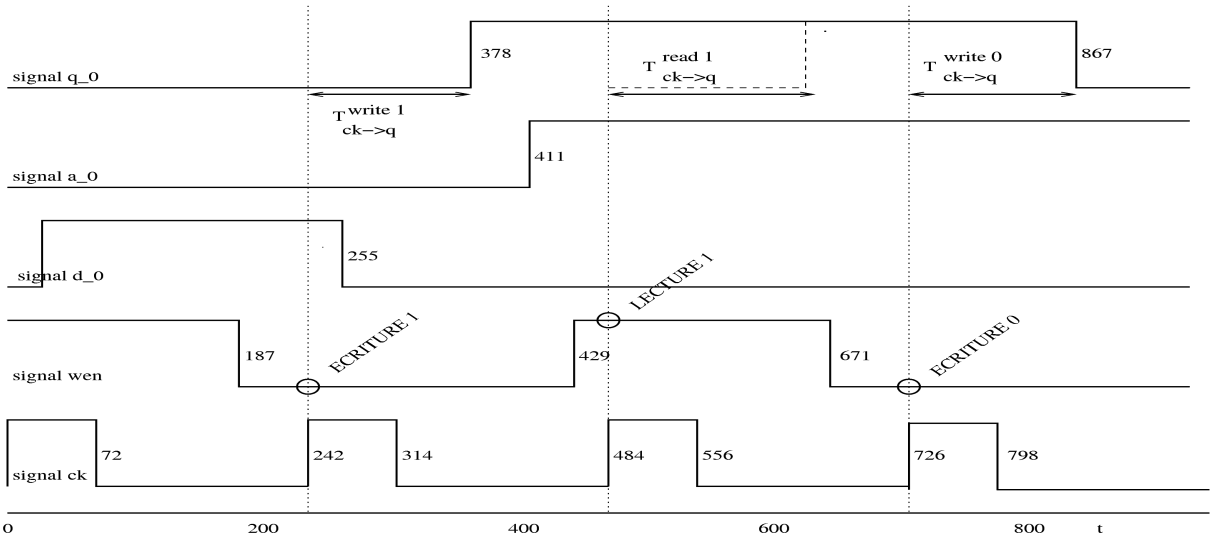
- Avec les délais de SP1:



Le graphe d'atteignabilité obtenu GA vérifie que :

GA |= A[] (((t > 385) imply q_0 == 0) and ((t > 166 and t < 385) imply q_0 == 1))
GA |/= A[] (((t > 386) imply q_0 == 0) and ((t > 166 and t < 386) imply q_0 == 1))

- Avec les délais de SP2:



Le graphe d'atteignabilité obtenu GA vérifie la première contrainte suivante :

A[] (((t > 867) imply q_0 == 0) and ((t > 378 and t < 867) imply q_0 == 1))

et il ne vérifie pas la contrainte :

A[] (((t > 868) imply q_0 == 0) and ((t > 378 and t < 868) imply q_0 == 1))

Comme on voit les résultats de tests sont bien conformes à ce qu'on a attendu. En ce qui concerne l'implémentation SP1 (l'implémentation SP2), tous les temps de réponse de l'opération d'écriture des valeurs 0 et 1, notée t_write(0) et t_write(1), sont égaux respectivement aux valeurs 56 (136) et 55 (141) qui vérifient la propriété du temps de réponse t_write ≤ t_write_max = 56 (141), où t_write_max dénote le temps maximum nécessaire pour l'opération d'écriture sur la sortie q. Comme on voit sur les chronogrammes, les contraintes ci-dessus sont vérifiées pour les valeurs optimales des temps setup t_setupd = 96 (229), t_setupwen = 29 (55) , t_setupa = 31 (73), associées aux signaux d'entrée D, WEN et A.

Les résultats obtenus et leur comparaison avec celles cités dans [CEFX 06a], sont récapitulés dans les tables mentionnées ci-dessous. On note que l'unité de temps est de 10 ps.

- Pour la l'implémentation SP1:

computed response time	value of the datasheet
$t^{read}_{CK\rightarrow Q} = 74$	$t^{read}_{max} == 77$
$t^{write}_{CK\rightarrow Q} = 56$	$t^{write}_{max} == 56$

Table 1.a : Temps de réponse pour SP1, obtenus dans [CEFX 06a].

computed response time
$t^{write}_{CK\rightarrow Q}(0) = 55$
$t^{write}_{CK\rightarrow Q}(1) = 56$

Table 1.b : Temps de réponse pour SP1, obtenus par l'outil.

setup parameter	optimal value obtained by computation	optimal value obtained by simulation	value of the datasheet
t^{D}_{setup}	95	95	108
t^{WEN}_{setup}	29	36	48
t^{A}_{setup}	31	30	58

Table 1.c : Temps de setup optimal pour SP1, obtenus dans [CEFX 06a].

setup parameter	optimal value obtained by the programme
t^{D}_{setup}	96
t^{WEN}_{setup}	29
t^{A}_{setup}	31

Table 1.d: Temps de réponse pour SP1, obtenus par l'outil.

- Pour la l'implémentation SP2:

computed response time	value of the datasheet
$t^{read}_{CK\rightarrow Q} = 169$	$t^{read}_{max} == 169$
$t^{write}_{CK\rightarrow Q} = 142$	$t^{write}_{max} == 142$

Table 2.a : Temps de réponse pour SP2, obtenus dans [CEFX 06a].

computed response time
$t^{write}_{CK\rightarrow Q}(0) = 141$
$t^{write}_{CK\rightarrow Q}(1) = 136$

Table 2.b : Temps de réponse pour SP2, obtenus par l'outil.

setup parameter	optimal value obtained by computation	optimal value obtained by simulation	value of the datasheet
t^{D}_{setup}	229	229	241
t^{WEN}_{setup}	55	55	109
t^{A}_{setup}	73	74	110

Table 2.c : Temps de setup optimal pour SP2, obtenus dans [CEFX 06a].

setup parameter	optimal value obtained by the programme
t^{D}_{setup}	229
t^{WEN}_{setup}	55
t^{A}_{setup}	73

Table 2.d: Temps de réponse pour SP2, obtenus par l'outil.

Il reste encore à tester d'autres environnements qui provoquent des lectures de 0 et 1 sur les points mémoires avec d'autres modèles vhdl, car le modèle lsv.vhd associée à l'architecture SPSMALL ne nous permet de voir bien ces lectures comme il n'a qu'un seul point mémoire sur lequel on effectue des lectures et écritures. Pour cela, on reprend l'architecture présenté dans [CEFX 06c] qui est une extension de l'architecture précédente avec deux points mémoires. On nomme le modèle VHDL associé à cette dernière architecture LSV2. Le AFTG associée à l'implémentation SP1 de cette architecture est donnée sur la figure 6.

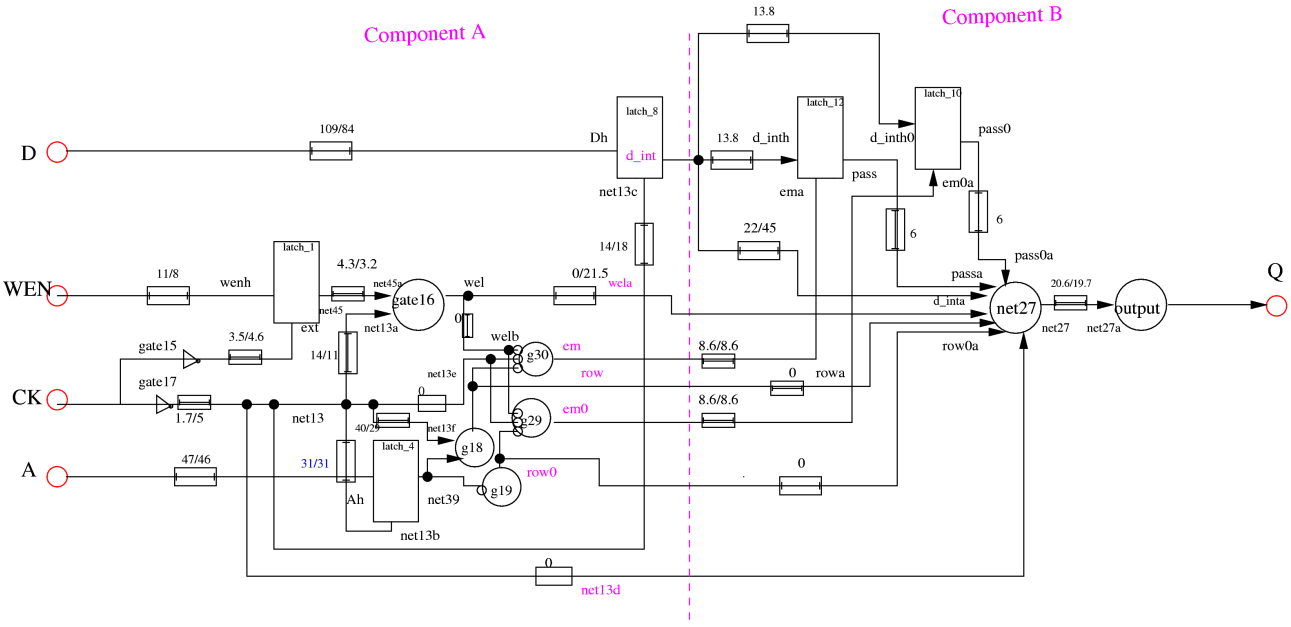


Figure 2: AFTG de l'extenssion de l'architecture SPSMALL avec deux points mémoires ([CEFX 06c])***.***

2.2. La description LSV2 :

Le programme VHDL qui implémente le circuit mentionné ci-dessus est donnée comme suit :

```
-- description SPSMALL selon BLUEBERRIES
-- modifications pour incorporer les délais dans les portes
--    - net13 supprime : gate 17 repliquee et delai de fils sur sortie
incorpores
--    - wel supprime : gate 9 repliquee et delai de fil de sortie incorpores
--    - delai 19 (fil de sortie) incorpore dans gate 14
--    - delai 20 incorpore dans gate 12
--    - delai 3 incorpore dans gate 15

ENTITY SPSMALL_BLUEBERRIES IS
  PORT (
         Q_0 : out   BIT;
          CK : in    BIT;
         WEN : in    BIT;
         A_0 : in    BIT;
         D_0 : in    BIT
  );
END SPSMALL_BLUEBERRIES;

-- Architecture Declaration

ARCHITECTURE RTL OF SPSMALL_BLUEBERRIES IS
  SIGNAL D_h : BIT;                 -- entree data latchD
  SIGNAL WEN_h : BIT;               -- entree data latchWEN
  SIGNAL A_h : BIT;                 -- entree data latchA
-- SIGNAL net13 : BIT;              -- le fameux signal net13
  SIGNAL en_latchWEN : bit;         -- enable de latchWEN, nommé enable_ext
  SIGNAL en_latchA : bit;           -- enable de latchA, aussi nommé net13b
  SIGNAL en_latchD : bit;           -- enable de latchD, aussi nommé net13c
  SIGNAL D_int : bit;               -- sortie latchD
  SIGNAL net45 : bit;               -- sortie latchWEN
  SIGNAL net39 : bit;               -- sortie latchA
  SIGNAL net13a : bit;              -- retard net13
  SIGNAL net13d : bit;              -- retard net13
  SIGNAL net13e : bit;              -- retard net13
  SIGNAL net13f : bit;              -- retard net13
  SIGNAL net45a : bit;              -- retard net45
--  SIGNAL wel : bit;               -- sortie gate 9
  SIGNAL wela : bit;                -- retard wel
  SIGNAL welb : bit;                -- retard wel
  SIGNAL row : bit;                 -- sortie gate 12
--  SIGNAL em : bit;                -- sortie gate 14
  SIGNAL ema : bit;                 -- sortie gate 14
  SIGNAL D_inta : bit;              -- retard D_int
  SIGNAL D_int_h : bit;             -- retard D_int
  SIGNAL rowa : bit;                -- retard row
  SIGNAL pass : bit;                -- sortie point memoire
  SIGNAL passa : bit;               -- retard pass
  SIGNAL net27 : bit;               -- retard pass
BEGIN

  D_h <= D_0;                       -- chaine d'inverseurs : delai 1
  A_h <= A_0;                       -- chaine d'inverseurs : delai 5
  WEN_h <= WEN;                     -- chaine d'inverseurs : delai 2

  -- net13 <= not CK;               -- gate 17 / delai 4
  en_latchWEN <= not CK;            -- gate 15 / delai 3
  en_latchA <= not CK;              -- delai 4 (not 17) +  delai 8 (retard)
```

```
  en_latchD <= not CK;              -- delai 4 (not 17) +  delai 16 (retard)

  net13a <= not CK;                 -- delai 4 (not 17) +  delai 7 (retard)
  net13d <= not CK;                 -- delai 4 (not 17) +  delai 23 (retard)
  net13e <= not CK;                 -- delai 4 (not 17) +  delai 26
  net13f <= not CK;                 -- delai 4 (not 17) +  delai 29

  net45a <= net45;                  -- retard / net45a / delai 28

  -- wel <= net45a or net13a;       -- gate 9 / PAS DE DELAI
  wela <= net45a or net13a;         -- delai nul (or 9) + delai 13
  welb <= net45a or net13a;         -- delai nul (or 9) + delai 11

   row <= net13f or net39;          -- gate 12 / PAS DE DELAI
   row0 <= net13f or not net39;           -- gate 12' / PAS DE DELAI

  -- em <= not (welb or net13e or row); -- gate 14 / PAS DE DELAI
  -- em0 <= not (welb or net13e or row0); -- gate 14 / PAS DE DELAI

  D_inta <= D_int;                  -- retard / D_inta / delai 18

  rowa <= net13f or net39;          -- delai nul (or 12) +  delai 20
  row0a <= net13f or not net39;           -- delai nul (or 12) +  delai 20

  ema <= not ((welb or net13e) or row);  -- delai nul (nor 14) +  delai 19
  em0a <= not ((welb or net13e) or row); -- delai nul (nor 14') +  delai 19 '

  passa <= pass;              -- retard / passa / delai 22
  pass0a <= pass0;                  -- retard / pass0a / delai 22'

  D_int_h <= D_int;                 -- retard / D_int_h / delai 17
  D_int_h0 <= D_int;                -- retard / D_int_h0 / delai 17'

  Q_0 <= net27;                     -- retard / net27a / delai 27

-- les process


  REG_latchD: PROCESS (en_latchD, D_h)   -- latchD / delai 15
      begin
      if en_latchD = '1' then
         D_int <= D_h;
      end if;
      end process;

  REG_latchWEN: PROCESS (en_latchWEN,WEN_h)-- latchWEN / delai 6
      begin
      if en_latchWEN = '1' then
         net45 <= WEN_h;
      end if;
      end process;

  REG_latch_A: PROCESS (en_latchA,A_h)   -- latchA / delai 10
      begin
      if en_latchA = '1' then
         net39 <= A_h;
      end if;
      end process;

  REG_mem_point: PROCESS (ema, D_int_h) -- point memoire / delai 21
      begin
      if ema = '1' then
```

```
        pass <= D_int_h;
      end if;
      end process;

  REG_mem_point0: PROCESS (em0a, D_int_h0) -- point memoire / delai 21 '
      begin
      if em0a = '1' then
        pass0 <= D_int_h0;
      end if;
      end process;

  REG_mux_output: PROCESS (passa, pass0a, D_inta, wela, rowa, row0a , net13d)
      begin                    -- mux et buffer de sortie / PAS DE DELAI
      if net13d = '0' and wela = '0' then
         net27 <= D_inta;
      elsif (wela = '1' and rowa = '0') then
         net27 <= passa;
      elsif (wela = '1' and row0a = '1') then
         net27 <= pass0a;

      end if;
      end process;
END;
```

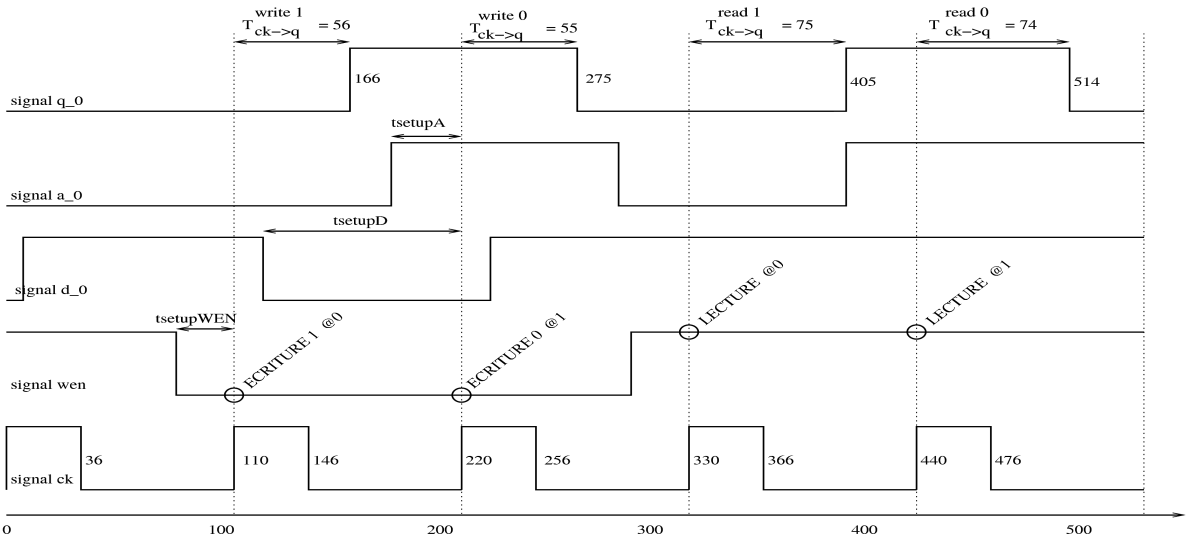
Les descriptions en hytech ou en uppaal, associées à ces implémentations SP1 et SP2, générées par la programme contiennent :

- 2026 lignes dans la description en hytech et 1723 lignes dans la description en uppaal.
- 34 automates (sans compter l'automate d'environnement).
- 35 horloges.
- 35+4 variables discrètes.
- 78 Paramètres.

A partir de la description uppaal générée, on peut tester des environnements d'écriture et lecture des valeurs 0 et 1 sur et à partir des deux points mémoires du modèle VHDL. Jusqu'à présent, on avait testé un seul environnement qui induit une écriture de 1 sur le premier point mémoire et 0 sur le deuxième point, suivies d'une lecture de chaque contenue de ces points, tout en respectant l'ordre de l'écriture, afin de voir bien les valeurs lues sur le sortie q_0. On va prendre en compte les deux implémentations précédents SP1 et SP2.

Environnement 1:

- Implementation SP1:



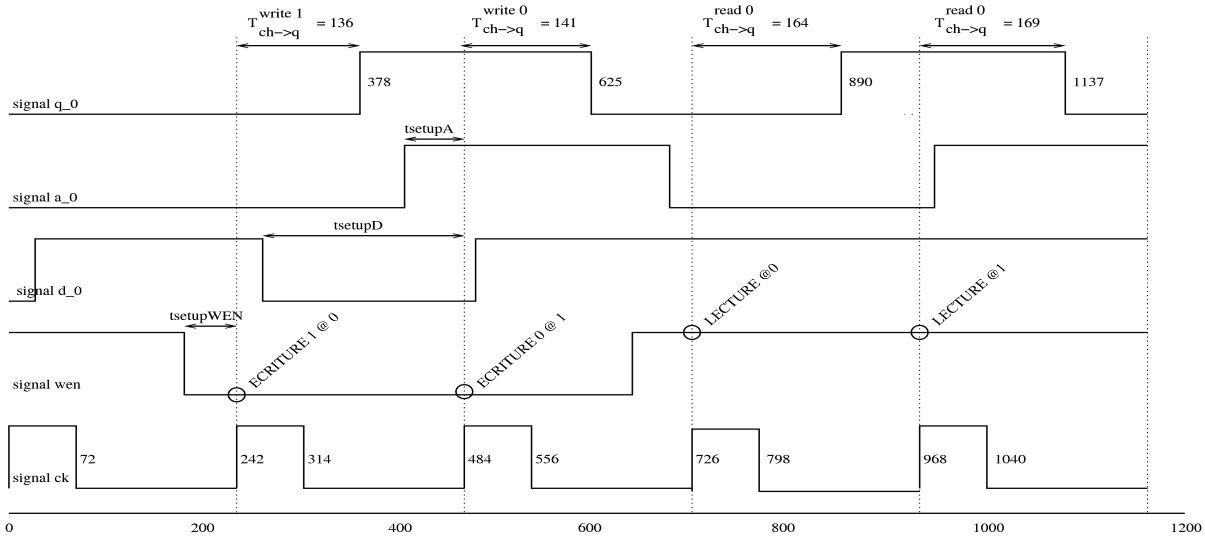
Le graphe d'atteignabilité obtenu GA vérifie la propriété.

A[] ((((t > 275 and t < 405) or (t > 514)) imply q_0 == 0) and
(((t > 166 and t < 275) or (t > 405 and t < 514)) imply q_0 == 1)
)

Bien qu'il ne vérifie pas :

A[] ((((t > 275 and t < 405) or (t > 515)) imply q_0 == 0) and
(((t > 166 and t < 275) or (t > 405 and t < 515)) imply q_0 == 1)
)

- Implementation SP2:



Le graphe d'atteignabilité obtenu GA vérifie la propriété.

A[] ((((t > 625 and t < 890) or (t > 1137)) imply q_0 == 0) and
(((t > 378 and t < 625) or (t > 890 and t < 1137)) imply q_0 == 1)
)

Bien qu'il ne vérifie pas :

A[] ((((t > 625 and t < 890) or (t > 1138)) imply q_0 == 0) and
(((t > 378 and t < 625) or (t > 890 and t < 1138)) imply q_0 == 1)

)

On peut encore remarquer facilement que les temps de lecture et d'ecritue sur la sortie q_0 correspondent parfaitement à ce qu'on avu dans [CEFX.06a & CEFX.06c]. En considérant l'implémentation SP1 (SP2), on a pour les valeurs du temps de setup : t_setupA ∈ {58, . . . , 34} ({110, . . . , 73}), t_setupD ∈ {108, . . . , 96} ({241, . . . , 229}), t_setupWEN ∈ {48, . . . , 29} ({109, . . . , 55}), les temps de réponses pour les commandes de lecture de 0 t_read0 = 74, de lecture de 1 t_read1 = 75, d'écriture de 0 t_write0 = 55 et d'écriture de 1 t_write1 = 56.

Par contre pour les valeurs des temps t_setupA = 33 (72) ou t_setupWEN = 28 (54), la propriété présenté ci-dessus n'est pas vérifiée sur tous les chemins. Ceci est dû à l'apparition simultané des signaux d'entrée *en_latchA* et *a_h* du latch *latch_A* (*en_latchWEN* et *WEN_h* du *latch_WEN*) qui peut induire deux valeurs différentes sur la sortie du latch (soit la sortie prend la nouvelle valeur, ou soit-même). En conséquence, des chemins qui ne satisfait la propriété peuvent être apparues. Donc, on doit ajouter toujours une unité de temps dans les sous expressions de l'expression, qui contient des délais des latch sur lequel se propage le signal d'entrée.

Les résultats obtenus et leur comparaison avec celles cités dans [CEFX 06a], sont aussi récapitulés dans les tables mentionnées ci-dessous. On rappelle que que l'unité de temps est de 10 ps.

- Pour la l'implémentation SP1:

computed response time	value of the datasheet
$t^{read}_{CK\rightarrow Q} = 74$	$t^{read}_{max} == 77$
$t^{write}_{CK\rightarrow Q} = 56$	$t^{write}_{max} == 56$

Table 3.a : Temps de réponse pour SP1, obtenus dans [CEFX 06a].

computed response time	
$t^{write}_{CK\rightarrow Q}(0) = 55$	$t^{read}_{CK\rightarrow Q}(0) = 74$
$t^{write}_{CK\rightarrow Q}(1) = 56$	$t^{read}_{CK\rightarrow Q}(1) = 75$

Table 3.b : Temps de réponse pour SP1, obtenus par l'outil.

setup parameter	optimal value obtained by computation	optimal value obtained by simulation	value of the datasheet
t^{D}_{setup}	95	95	108
t^{WEN}_{setup}	29	36	48
t^{A}_{setup}	31	30	58

Table 3.c : Temps de setup optimal pour SP1, obtenus dans [CEFX 06a].

setup parameter	optimal value obtained by the programme
t^{D}_{setup}	96
t^{WEN}_{setup}	29
t^{A}_{setup}	34

Table 3.d : Temps de réponse pour SP1, obtenus par l'outil.

- Pour la l'implémentation SP2:

computed response time	value of the datasheet
$t^{read}_{CK\rightarrow Q} = 169$	$t^{read}_{max} == 169$
$t^{write}_{CK\rightarrow Q} = 142$	$t^{write}_{max} == 142$

Table 4.a : Temps de réponse pour SP2, obtenus dans [CEFX 06a] & [Xu 06].

computed response time	
$t^{write}_{CK\rightarrow Q}(0) = 141$	$t^{read}_{CK\rightarrow Q}(0) = 169$
$t^{write}_{CK\rightarrow Q}(1) = 136$	$t^{read}_{CK\rightarrow Q}(1) = 164$

Table 4.b : Temps de réponse pour SP2, obtenus par l'outil.

setup parameter	optimal value obtained by computation	optimal value obtained by simulation	value of the datasheet
t^{D}_{setup}	229	229	241
t^{WEN}_{setup}	55	55	109
t^{A}_{setup}	73	74	110

Table 4.c : Temps de setup optimal pour SP2, obtenus dans [CEFX 06a] & [Xu 06].

setup parameter	optimal value obtained by the programme
t^{D}_{setup}	229
t^{WEN}_{setup}	55
t^{A}_{setup}	73

Table 4.d : Temps de réponse pour SP2, obtenus par l'outil.

3. La description VHDL de Pirouz modifiée (SP_1x2):

Les deux descriptions en hytech suivantes sont générées à partir de la description en VHDL sp_1x2_md_.vhd.

3.1. La description sp_1x2_md_no.hy (sans optimisation) :

Elle est générée avec les options :

- version éclatées: non.
- optimisation des gardes simples : non.
- optimisation de la figure : non.

La description contient :

- 5771 lignes.
- 90 automates (l'automate d'environnement inclus aussi).
- 90 horloges.
- 80 + 15 (i_B) + 17 (B_i) = 112 variables discrètes.
- 178 Paramètres.

- Resultats d'analyse avec Hytech :

```
Checking automaton P_pr15
Checking automaton B2_pr15
Checking automaton B1_pr15
Checking automaton P_pr16
Checking automaton B2_pr16
Checking automaton B1_pr16
Checking automaton Ass_v_18_f_net83
Checking automaton Ass_v_18_f_i47_oe_local_h
Checking automaton Ass_v_18_f_data_delay_h
Checking automaton Ass_v_18_f_clk_local_l

Checking automaton Ass_v_18_f_net81
Checking automaton Ass_v_18_e_clk_local_l
Checking automaton Ass_v_18_e_net81
Checking automaton Ass_v_18_e_i47_oe_local_h
Checking automaton Ass_v_18_e_data_delay_h
Checking automaton Ass_v_18_e_net83
Checking automaton Ass_v_17_12_10_net96
Checking automaton Ass_v_17_12_10_net115
Checking automaton Ass_v_17_12_10_we_latched_h
Checking automaton Ass_v_17_12_10_net100

Checking automaton Ass_v_17_12_10_ext_we_h
Checking automaton Ass_v_17_12_11_i62_a_delay_h
Checking automaton Ass_v_17_12_11_i62_net53
Checking automaton Ass_v_17_12_11_net120
Checking automaton Ass_v_17_12_11_i63_a_delay_h
Checking automaton Ass_v_17_12_11_i63_net53
Checking automaton Ass_v_17_12_11_net54
Checking automaton Ass_v_18_f_net85
Checking automaton Ass_v_18_e_net85
Checking automaton P_pr5

Checking automaton B1_pr5
Checking automaton Ass_v_18_f_clk_local_h
Checking automaton Ass_v_18_e_clk_local_h
Checking automaton P_pr6
Checking automaton B1_pr6
```

```
Checking automaton Ass_v_17_12_10_ext_cs_h
Checking automaton Ass_v_17_12_11_net58
Checking automaton Ass_v_17_12_11_add01
Checking automaton Ass_v_17_12_10_net202
Checking automaton Ass_v_18_f_bit_l_inv

Checking automaton Ass_v_18_e_bit_l_inv
Checking automaton Ass_v_16_13_a1
Checking automaton Ass_v_17_12_10_net127
Checking automaton Ass_v_17_12_10_net113
Checking automaton Ass_v_16_13_net25
Checking automaton Ass_v_16_13_a1inv
Checking automaton Ass_v_17_12_10_we_l
Checking automaton P_pr7
Checking automaton B1_pr7
Checking automaton P_pr8

Checking automaton B1_pr8
Checking automaton Ass_row
Checking automaton Ass_v_17_12_10_net41
Checking automaton Ass_v_17_12_11_dec_eval0_l
Checking automaton Ass_v_17_12_clk_sig_h
Checking automaton Ass_clk_h
Checking automaton P_pr9
Checking automaton B1_pr9
Checking automaton P_pr10
Checking automaton B1_pr10

Checking automaton P_pr11
Checking automaton B1_pr11
Checking automaton P_pr12
Checking automaton B1_pr12
Checking automaton P_pr13
Checking automaton B1_pr13
Checking automaton P_pr14
Checking automaton B1_pr14
Checking automaton Ass_dec_0
Checking automaton Ass_v_17_12_10_net13

Checking automaton Ass_we_h
Checking automaton Ass_oe_l
Checking automaton P_pr17
Checking automaton B1_pr17
Checking automaton P_pr18
Checking automaton B1_pr18
Checking automaton Ass_v_18_f_i47_out_n_drive_h
Checking automaton Ass_v_18_e_i47_out_n_drive_h
Checking automaton Ass_v_18_f_i47_out_p_drive_l
Checking automaton Ass_v_18_e_i47_out_p_drive_l

Checking automaton P_pr19
Checking automaton B1_pr19
Checking automaton Ass_v_19_9_pass_l
Checking automaton Ass_v_19_8_pass_l
Checking automaton Ass_v_19_8_pass_h
Checking automaton Ass_b_0_0
Checking automaton Ass_b_0_1
Checking automaton Ass_b0
Checking automaton Ass_b1
Checking automaton env

 WARNING: locn env_init of automaton env has no incoming transitions
```

Error. too many vars
Exceeds limit of 150

3.2. La description sp_1x2_md.hy (avec optimisation de la figure et des gardes simples des processus):

Elle est générée avec les options :

- version éclatée : non.
- optimisation des gardes simples : oui.
- optimisation de la figure : oui.

La description contient :

- 4751 lignes.
- 56 automates (l'automate d'environnement inclus aussi).
- 56 horloges.
- 58 + 5 (i_B) + 5 (B_i) = 68 variables discrètes.
- 178 Paramètres.

Les signaux auxilières réduits sont données comme suit :

signal v_17_12_10_net8
signal v_17_12_11_i62_net39
signal v_17_12_11_i63_net39
signal v_17_12_10_net45
signal v_17_12_10_clk_ext_delay_1
signal v_16_15_a1
signal v_16_14_a1
signal v_16_15_net25
signal v_16_14_net25
signal v_16_15_a1inv
signal v_16_14_a1inv
signal v_17_add_en_h
signal v_17_add_en_1
signal v_17_12_11_dec_eval1_1
signal v_17_12_11_dec_eval2_1
signal v_17_12_11_dec_eval3_1
signal dec_1
signal dec_2.

Resultats d'analyse avec Hytech :

```
Checking automaton P_pr15
Checking automaton P_pr16
Checking automaton Ass_v_18_f_i47_oe_local_h
Checking automaton Ass_v_18_f_data_delay_h
Checking automaton Ass_v_18_f_clk_local_l
Checking automaton Ass_v_18_e_clk_local_l
Checking automaton Ass_v_18_e_i47_oe_local_h
Checking automaton Ass_v_18_e_data_delay_h
Checking automaton Ass_v_17_12_10_we_latched_h
Checking automaton Ass_v_17_12_10_ext_we_h

Checking automaton Ass_v_17_12_11_i62_a_delay_h
Checking automaton Ass_v_17_12_11_i63_a_delay_h
Checking automaton P_pr5
Checking automaton Ass_v_18_f_clk_local_h
Checking automaton Ass_v_18_e_clk_local_h
Checking automaton P_pr6
Checking automaton Ass_v_17_12_10_ext_cs_h
Checking automaton Ass_v_17_12_11_net58
Checking automaton Ass_v_17_12_11_add01
```

```
Checking automaton Ass_v_18_f_bit_l_inv

Checking automaton Ass_v_18_e_bit_l_inv
Checking automaton Ass_v_17_12_10_we_l
Checking automaton P_pr7
Checking automaton B1_pr7
Checking automaton P_pr8
Checking automaton B1_pr8
Checking automaton Ass_row
Checking automaton Ass_v_17_12_11_dec_eval0_l
Checking automaton Ass_v_17_12_clk_sig_h
Checking automaton P_pr9

Checking automaton P_pr10
Checking automaton P_pr11
Checking automaton P_pr12
Checking automaton P_pr13
Checking automaton P_pr14
Checking automaton Ass_v_17_12_10_net13
Checking automaton Ass_we_h
Checking automaton Ass_oe_l
Checking automaton P_pr17
Checking automaton B1_pr17

Checking automaton P_pr18
Checking automaton B1_pr18
Checking automaton Ass_v_18_f_i47_out_n_drive_h
Checking automaton Ass_v_18_e_i47_out_n_drive_h
Checking automaton Ass_v_18_f_i47_out_p_drive_l
Checking automaton Ass_v_18_e_i47_out_p_drive_l
Checking automaton P_pr19
Checking automaton B1_pr19
Checking automaton Ass_v_19_9_pass_l
Checking automaton Ass_v_19_8_pass_l

Checking automaton Ass_v_19_8_pass_h
Checking automaton Ass_b_0_0
Checking automaton Ass_b_0_1
Checking automaton Ass_b0
Checking automaton Ass_b1
Checking automaton env

 WARNING: locn env_init of automaton env has no incoming transitions
Error. too many vars
Exceeds limit of 150
```

Comme on voit, les deux descriptions Hytech sont syntaxiquement correctes. Malheureusement,elles ne passent pas vers la phase d'analyse car on atteint jamais la fin d'analyse comme le nombre de variables est important. En revanche les descriptions en Uppaal associées, passent bien sur l'outil Uppaal. Ce dernier réussit bien à construire le graphe d'atteignabilité, et d'explorer tous les états du graphe, en moins d'une minute, afin de vérifier une propriété CTL donnée dont le connecteur principal est le connecteur temporel AG.