Remy Chevallier
042/63/25
eSRAM team / Crolles1

1.Goal of the meeting

- Status on VALMEM project
- LIP6 : Temporal extraction integration (Pirouz/Patricia/Dominique)
- 3.2.LIP6: VHDL2TA: Automated translation of VDHL with timings into timed automaton format (HyTech/Uppaal) (Abdelrezzak/Emmanuelle)
- LSV: Parameterize model: From IMITATOR to IMITATOR2 (Etienne/Laurent)
- Publication status

2.Attendees

Emmanuelle Encrenaz	LIP6
Abdelrezzak Bara	LIP6
Pirouz Bazargan-Sabet	LIP6
Dominique Ledu	LIP6
Laurent Fribourg	LSV
Etienne André	LSV
Remy Chevallier	ST

3.Summary of the meeting

3.1.LIP6: Temporal extraction integration

LIP6 is developing a tool which allows, from a spice netlist, the abstraction of the functionality based on elementary bricks (in VHDL language) and the computation of the delay for each brick.
The abstraction tool is finished and work properly on SPSMALL testcase. The LIP6 team is focusing on timing computation:

- The temporal delay is computed with spice simulations on each elementary brick:
  - The full cell with the load (RC network + input transistors of next tool) is simulated
  - When there are conflicts or latches/flipflop the complete logic must be included. Today, it is not the case then the delays are over estimated

Improvement:

- Delays for all gates of SPSMALL3x2 have been generated.

Next steps:

- Compare delay of the model with the delay provided by the tool. This description will be used by LSV tool after translation by VHDL2TA tool.
- Improved the delay with the generation of the netlist for conflict cells and run the spice simulation to improve the timing accuracy
- Push the limit of the tool with various size of SPSMALL memory
- Study the SPREG

3.2.LIP6: VHDL2TA: Automated translation of VDHL with timings into timed automaton format (HyTech/Uppaal)

The goal of this tool is to translate VHDL netlist and timings provided by abstraction tool into timed automaton formalism. The presentation and demonstration of this new tool has been done during the meeting. The current status is the following:

- VHDL and timings as inputs are supported. Generation of automaton for Hytech and Uppaal formal tool is supported:
  - SPSMALL modeling: the optimized performances catch manually in Blueberries project has been reached with the automated tool
  - FlipFlop modeling (cotadella): issue founds during the meeting: a dedicated meeting will be done
  - Andor modeling (cotadella): issue founds during the meeting: a dedicated meeting will be done
  - BRO1 and BRO2 (digital design founds in Brozowski book) are modeled and verified
- Functionality constraints are generated by an 'environment file'. This file is very useful to constraint the clock, reset…. For the formal verification.

All the generation and verifications are performed in few seconds.

Next steps:

- 8 automaton from SPSMALL are not supported today: check if they can be supported
- Verify a FIFO
- Verify Ring Oscillator Rambus

3.3.LSV: Parameterize model: From IMITATOR to IMITATOR2

Hytech formal tool is used in IMITATOR: It generates the full reachable states before removing the unreachable elements due to user constraints.
For SPSMALL, the generation of the full environment takes 99% of the time (87minutes) and the verification itself takes few minutes.
→ IMITATOR2: generate the reachable states on the fly: the unused states are not generated.
First results expected by the end of December.
The development of this new engine is ongoing.

3.4.Visit at ST

- In the project, a visit at ST was planned. The agenda and the visit has to be discussed. The following proposal has been discussed
  - Abstraction:
    - Presentation of VALMEM work
    - Deep study of SPREG with Remy/designers
  - Verification
    - To be define
  - Budget evaluation
  - Define a planning/program: End of November (wk49)

3.5.Cassandra ANR prject submission status

- The project has been rejected
- The main weaknesses underlines by the reviewer are:
  - Why are we focusing on NBTI
  - The state of art task should be removed because the reviewer is underlining that the state of art is already done for the project submission
- Check with Vincent Huard if he what to continue on our Cassandra project

4.Publications

4.1.Current publications

- Etienne André, Thomas Chatain, Emmanuelle Encrenaz and Laurent Fribourg. **An Inverse Method for Parametric Timed Automata**. International Journal of Foundations of Computer Science, 2009.
- Etienne André, Thomas Chatain, Emmanuelle Encrenaz, Laurent Fribourg. **An Inverse Method for Parametric Timed Automata**. *In* Vesa Halava and Igor Potapov (eds.), RP'08, ENTCS 223, pages 29-46. Elsevier Science Publishers, 2008

4.2.Target

4.2.1.Abstraction

- Exploration of the transistor network with color algorithm (Dec 2009)
- Functional analysis for conflict (Mars 2010)
- Loop analysis (Mars 2010)

4.2.2.Abstraction and timing

- Translation of VHDL + timing to formal automaton analysis → Targeting RSP conf (dead line in January)

4.2.3.Formal analysis

- Have to finalize IMITATOR2 to evaluate the possible publications (Finalize INITATOR2 tool for end of January for SPSMALL1x2)

4.2.4.Abstraction, Timing and Formal analysis

- Build a complete paper with all the steps built in VALMEM (ie: ASPDAC: April/May 2010)

5.Actions

- Administrative
  - Follow-up the 'Accord de consortium' story (All) [asap]
- Compare full memory simulation timings for SPSMALL with simulation performed brick by brick with the abstraction tool (LIP6)
- Provide the timing for translation and verification with VHDL2TA tool (LIP6)
- Run verification on SPSMALL with real timings

- IMITATOR2 development (LSV) [end of January]
- Publication
  - Based on current results with VHDL2TA, a paper will be written for RSP conference (LIP6) [end of January]

6.Next meeting

The next meeting is planned in LIP6 at the beginning of February.

7.Deliverable overview

No.	Title	Deliv.	Resp.	Target	status
D1.1	State of Art in eSRAM conception	R	ST	0→6	Done
D1.2	Build web site for the project	R	LIP6	0→6	Done
D1.3	Description of the conception flow applied on a study	R	ST	6→12	Study 1 done Study 2 done Study 3 not started Run time of conception flow done
D2.1	State of art in memory verification methodologies	R	LIP6	0→6	Done
D2.2	Definition of a new functional and timed model	R	LIP6	0→6	Done
D2.3	Mixing of abstraction methods and temporal characterization	R	LIP6	6→12	Done
D2.4	Abstraction tool prototype	P	LIP6	12→48	ongoing
D3.1	Temporal automaton modeling adapted to memory	R	LSV	6→12	Done
D3.2	Temporal automaton model checking adapted to memory	R	LSV	12→18	Done
D3.3	verification tool prototype	P	LSV	12→24	Done
~~D4.1~~	~~Description of the conception flow applied on other studies~~	~~R~~	~~ST~~	~~12→18~~	~~Not started~~
D4.2	Experimentation of prototypes on real study	R & D	ST	18→48	ongoing
D4.3	Comparison of results from current verification methods and new methods	R	ST	30→48	ongoing

The targets are described in months.
Delivery naming: (R: report / P: prototype / D: demonstrator)
wk: week number
Q: quarter